EE 231 - Homework 7

Due Oct. 12 2018

P5.8
(Consider the circuit shown below. Assume that the two NAND gates have much longer (about four times) propagation delay than the other gates in the circuit.

Simulate the circuit in Vivado and determine its behavior. Include your assumptions as well as the timing diagram.

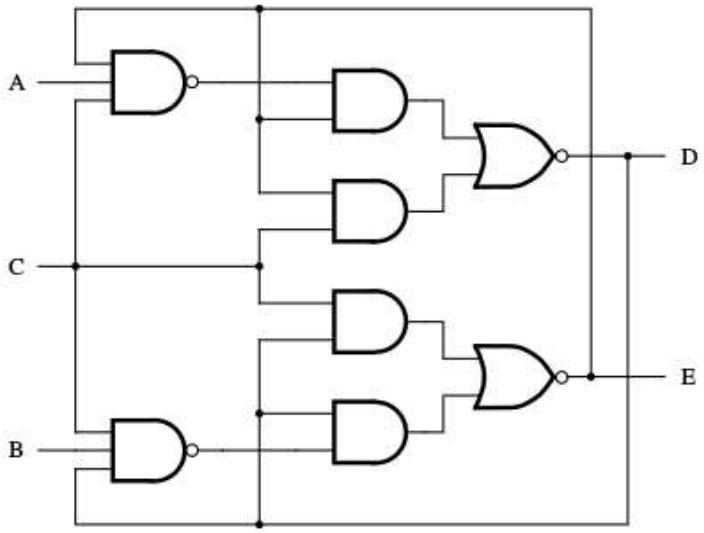

Figure P5.2 Circuit for Problem 5.8.