EE 231 - Homework 9

Due Nov. 2 2018

Design a counter as a finite state machine. The specification for the counter is

- The counting sequence is 0,1,2,3,0,1,... (modulo 4 counter)
- There exists an input signal w. The value of this signal is considered during each clock cycle. If $w = 0$, the present count remains the same; if $w = 1$, the count is incremented.

1. Implement the counter using D-Type Flip-Flops
2. Implement the counter using JK-Type Flip-Flops