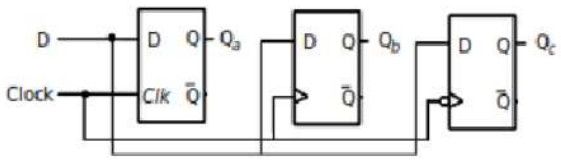
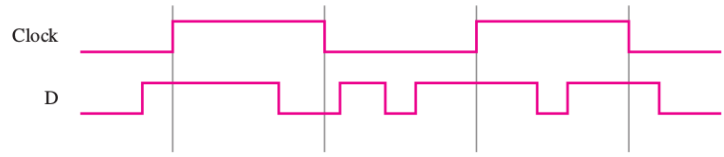
EE 231 - Homework 10

1. Consider the timing diagram below. Assuming that the D and $Clock$ inputs shown are applied to the adjunct circuit, draw waveforms for the Q_a, Q_b, and Q_c signals. Assume that the initial values for the flip-flops are $Q_a, Q_b, Q_c = 0, 0, 0$.





Qa_____

Qb_____

Qc_____

2. Describe the counting sequence of a T-flip-flop circuit with the following interconnections. Assume that the initial values of the flip-flops are $\{Q_3Q_2Q_1Q_0 = 1001\}$

   $T_3 = Q_3 \cdot Q_0 + Q_2 \cdot Q_1 \cdot Q_0$, $T_2 = Q_1 \cdot Q_0$, $T_1 = \overline{Q_3} \cdot Q_0$, $T_0 = 1$.

3. The program shown below describes a counter in Verilog. Assume that the initial values for the flip-flops are Q0,Q1,Q2,Q3=0,0,0,0. What is the counting sequence implemented by the code?

```
module counter(Clk, Resetn, Q);
    input Clk, Resetn;
    output reg [3:0] Q;

    always@(posedge Clk, negedge Resetn)
    if(!Resetn)
        Q<=0;
    else begin
        Q[3:1] <= Q[2:0];
        Q[0]   <= ~Q[3];
    end

endmodule
```

4. Derive a state diagram and a state table for a FSM that has an input **w** and an output **z**, such that when pulses are applied to **w**,

   (a) the output **z = 0** if the number of previously applied pulses is **odd** , and

   (b) the output **z = 1** if the number of applied pulses is **even**.

5. Design a 2-bit synchronous binary counter using D flip-flops, and find its maximum operating frequency. Assume the following timing parameters for the flip-flops: tsu=0.6 ns, th=0.4 ns, and 0.8 tcQ 1.0 ns, and that the delay through any logic gates can be calculated as 1+0.1k ns, where k is the number of inputs