EE 231 - Homework 12, due Nov. 28

Timing Analysis with Clock Skew A variation in the arrival time of a clock signal at different flip-flops is called **clock skew,** t_{skew}. For The circuit below, assume that:

$$t_{su} = 0.6 \quad ns, \quad t_h = 0.4 \quad ns, \quad and \quad 0.8 \leq t_{cQ} \leq 1.0 \quad ns.$$

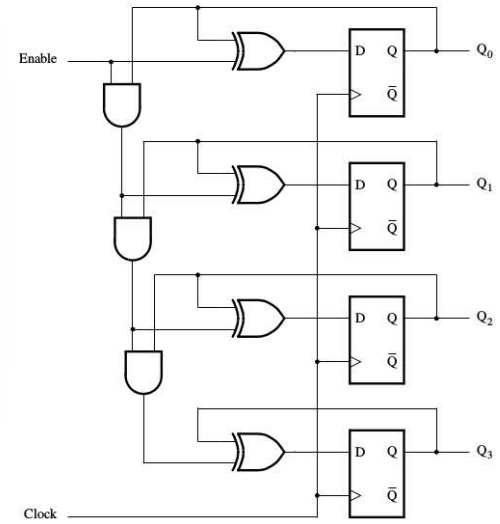

Figure 5.67 A 4-bit counter.

Assume that the clock signal arrives at flip-flops Q_0 , Q_1 , and Q_2 simultaneously, but that there is a delay in the arrival of the clock signal at flip-flop Q_3.

1. The critical path through the circuit is from flip-flop Q_0 to Q_3. **However**, the clock skew at Q_3 has the effect of **reducing** this delay, because it provides additional time before data is loaded into this flip-flop. Thus, taking a clock skew of $t_{skew} = 1.5$ ns into account, the delay of the path from flip-flop Q_0 to Q_3 is given by

   $$t_{cQ} + 3(t_{AND}) + t_{XOR} + t_{su} - t_{skew} = 4.9 \quad ns$$

   which in turn increases the maximum clock operating frequency.

   Can we come up with a (better than the authors') explanation of why the delay reduction occurs?

2. Since the loading of data into flip-flop Q_3 is delayed by the clock skew, it has the effect of **increasing** the hold time requirement of this flip-flop to

   $$t_h + t_{skew} (= 1.9ns),$$

   for all paths that end at Q_3 but start at Q_0 ,Q_1 , or Q_2. The shortest such path in the circuit is from flip-flop Q_2 to Q_3 and has the delay

   $$t_{cQ} + t_{AND} + t_{XOR} = 0.8 + 1.2 + 1.2 = 3.2 \quad ns.$$

   (which is still larger than 1.9 ns. so, no hold time violation occurs.)

   Can we come up with a (better than the authors') explanation for the increase in the hold time requirement ?

3. Finally, If we repeat the above hold time analysis for clock skew values

   $$t_{skew} \geq 3.2 - t_h = 2.8 \quad ns,$$

   then hold time violations will exist. Thus, **if** $t_{skew} \geq 2.8ns$ the circuit **will not work reliably at any clock frequency**. **Why is it so?**