Lab 6: Debouncing Switches

Introduction

Switches are mechanical devices, and as such, they are much slower than electronic circuits. When a switch is opened or closed the mechanical contacts do not break or make a connection instantaneously, but can "bounce" between open and closed, thus making several transitions. If one were to use a mechanical switch to increment a counter (to count, say, people going through a turnstile), a single closure of the switch could increment the counter many times for one single "Press". In this lab use the logic analyzer to look at switch bounce, and use an SR latch to debounce a mechanical switch.

1 Prelab

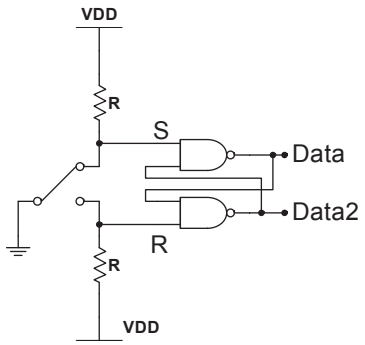


Figure 1: NAND Debounced Single-Pole Double-Throw (SPDT) Switch Circuit

1.1. The waveform shown in Figure 2 shows the values on S and R when the switch from Figure 1 is moved from the UP position to the Down position, then moved back to the UP position. Complete the timing diagram to show the expected values of Data (Top **NAND** gate; takes S as an input) and Data2 (Bottom **NAND** gate; takes R as an input) outputs.

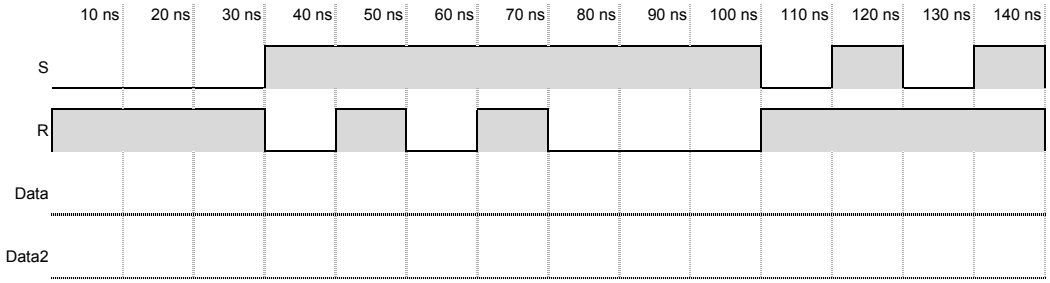


Figure 2: SR Latch Sample Input for Prelab

2 Lab

2.1 Switch Bounce

2.1.1. Build the switch in Figure 3. For now, just use a wire as the switch. Plug the wire into GND to bring `DATA` (the switch output) low, alternatively, unplug it to bring `DATA` high.

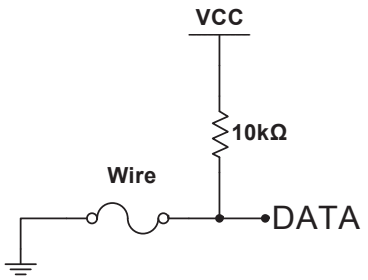


Figure 3: Simple Switch Circuit

2.1.2. Test the circuit with a logic probe and make sure it operates as described above.

2.1.3. Connect the output of the switch (`DATA`) to one channel of your logic analyzer. Start with your switch closed (wire attached to GND). Click on the play button, pull the wire out, and see if you can observe switch bounce.

2.1.4. If you could not see the switch bounce as described above, it's because the logic analyzer sampling period is so short that by the time you pulled out the wire of the "switch," the sampling period had ended.Because of this you were unable to observe the low-to-high transition of the switch. In order to observe this transition you need to have the logic analyzer sample for a longer period of time. Doing so will allow the logic analyzer to capture the transition, and you to observe the captured waveform.

2.1.5. Pull the wire from GND again. The logic analyzer should capture the transition, and display the switch bouncing.

2.1.6. Capture the waveform for several switch bounces.

2.1.7. **How many bounces do you typically get?**

2.1.8. **What is the typical length of a bounce?**

2.1.9. **From the initial low-to-high transition, how long does it take the switch to reach a constant high value?**

2.1.10. Repeat the above test with the switch initially in the open position (high-to-low).

2.2 Debouncing with an SR Latch

2.2.1. Build the circuit shown in Figure 1. Use 10kΩ resistors. Use a wire to simulate your switch.

2.2.2. Connect `S`, `R`, `Data` (`Q`,) and `Data2` (`Q'`) to the logic analyzer.

2.2.3. ⋆⋆ Observe the outputs when you toggle your switch.

2.2.4. **Does this circuit eliminate the bouncing?**

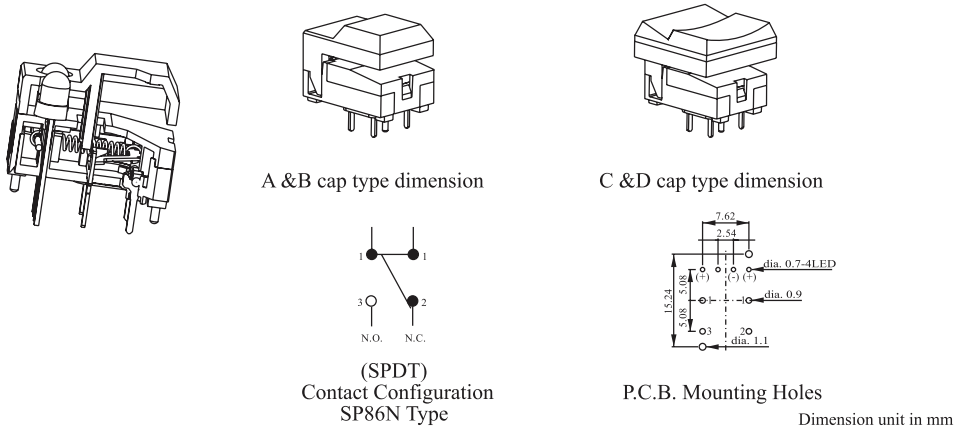
2.3 Build a Real Debounced Switch

2.3.1. The switch you are using is a single-pole double-throw switch as shown in Figure 4. When your switch is oriented with the hinge on the top:

- The common leads will be the two on top.
- With the switch un-depressed (unpressed), the closed lead is the on the right, with the normally open (N.O.) lead on the left.

2.3.2. Build a debounced switch circuit from Figure 1 using the SPDT Switch.

2.3.3. ⋆⋆ Again, observe your circuit using the logic analyzer. Does the NAND circuit debounce the switch?



http://www.cresttech.com.au/pdf/switches/SP86N.pdf

Figure 4: Excerpt from SP86N Series Datasheet