Homework 7: EE 252 Digital Electronics

5.14 Design a four-bit synchronous counter with parallel load. Use T flip-flops, instead of the D flip-flops used in Section 5.9.3

5.16 Repeat Problem 5.15 using D flip-flops. (***5.15** Design a three-bit up/down counter using T flip-flops. It should include a control input called Up/Down. If Up/Down = 0, then the circuit should behave as an up-counter. If Up/Down = 1, then the circuit should behave as a down-counter.)

5.18 Consider the circuit in Figure P5.4. How does this circuit compare with the circuit in Figure 5.16? Can the circuits be used for the same purposes? If not, what is the key difference between them?

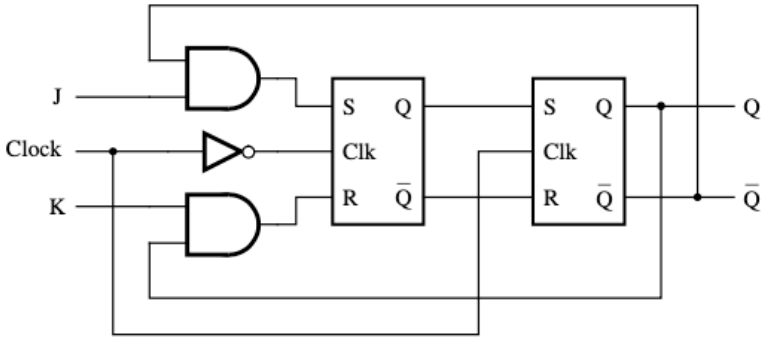

Figure P5.4 Circuit for Problem 5.18.

***6.2** Derive a circuit that realizes the FSM defined by the state-assigned table in Figure P6.1 using JK flip-flops.

Present state y_2y_1	Next state $w = 0$ Y_2Y_1	Next state $w = 1$ Y_2Y_1	Output z
0 0	1 0	1 1	0
0 1	0 1	0 0	0
1 0	1 1	0 0	0
1 1	1 0	0 1	1

Figure P6.1 State-assigned table for Problems 6.1 and 6.2.