## Homework 8: EE 252 Digital Electronics

1. Determine the expressions for $\mathbf{d}$ and $\mathbf{e}$ in terms of $\mathbf{a}, \mathbf{b}$ and $\mathbf{c}$.

2.- Determine the counting sequence for the Verilog code below, starting with the pattern 001
```
module counter (R, L, Clock, Q);
    input [0:2] R;
    input L, Clock;
    output reg [0:2] Q;
    always @(posedge Clock)
        if (L)
            Q < = R;
        else
            \(\mathrm{Q}<=\left\{\mathrm{Q}[2], \mathrm{Q}[0]^{\wedge} \mathrm{Q}[2], \mathrm{Q}[1]\right\} ;\)
endmodule
```

3.- Design a modulo-6 counter, which counts in the sequence $0,1,2,3,4,5,0,1, \ldots$ The counter counts the clock pulses if its enable input, $w$, is equal to 1 . Use $D$ flip-flops in your circuit.

