

Homework 5: EE 252 Digital Electronics

1. Determine the decimal values of the following unsigned numbers:

- (a) $(0111011110)_2$
- (b) $(1011100111)_2$
- (c) $(3751)_8$
- (d) $(A25F)_{16}$
- (e) $(F0F0)_{16}$

2. Determine the decimal values of the following 2's complement numbers:

- (a) 0111011110
- (b) 1011100111
- (c) 1111111110

3. Perform the following operations involving eight-bit 2's complement numbers and indicate whether arithmetic overflow occurs. Check your answers by converting to decimal sign- and-magnitude representation.

$\begin{array}{r} 00110110 \\ + 01000101 \\ \hline \end{array}$	$\begin{array}{r} 01110101 \\ + 11011110 \\ \hline \end{array}$	$\begin{array}{r} 11011111 \\ + 10111000 \\ \hline \end{array}$
$\begin{array}{r} 00110110 \\ - 00101011 \\ \hline \end{array}$	$\begin{array}{r} 01110101 \\ - 11010110 \\ \hline \end{array}$	$\begin{array}{r} 11010011 \\ - 11101100 \\ \hline \end{array}$

4. Show that the circuit in Figure 3.4 implements the full-adder specified in the Truth table below.

c_i	x_i	y_i	c_{i+1}	s_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(a) Truth table

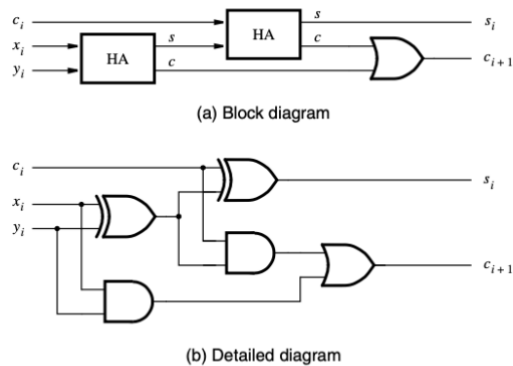


Figure 3.4 A decomposed implementation of the full-adder circuit.