Homework 7: EE 252 Digital Electronics

5.1 Consider the timing diagram in Figure P5.1. Assuming that the *D* and *Clock* inputs shown are applied to the circuit in Figure 5.10, draw waveforms for the Q_a, Q_b, and Q_c signals.

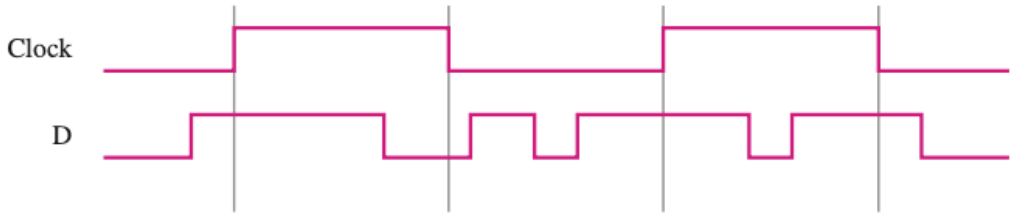
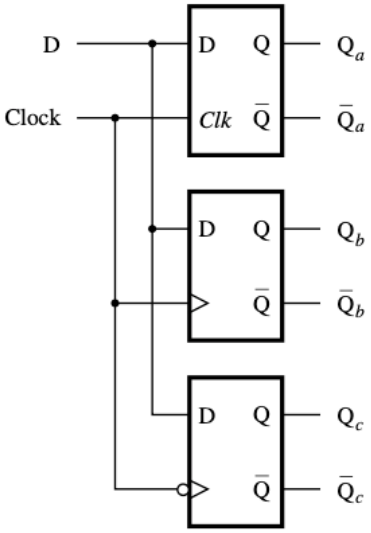


Figure P5.1 Timing diagram for Problem 5.1.



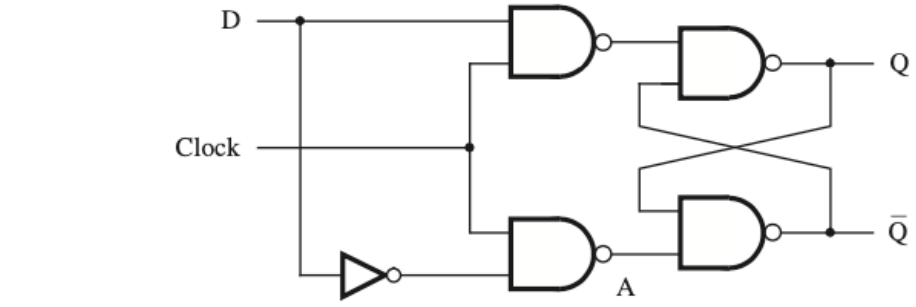
(a) Circuit

Figure 5.10 Comparison of level-sensitive and edge-triggered D storage elements.

5.4 Given a 100-MHz clock signal, derive a circuit using D flip-flops to generate 50-MHz and 25-MHz clock signals. Draw a timing diagram for all three clock signals, assuming reasonable delays.

5.12 A universal shift register can shift in both the left-to-right and right-to-left directions, and it has parallel-load capability. Draw a circuit for such a shift register.

5.25 A circuit for a gated D latch is shown in Figure P5.7. Assume that the propagation delay through either a NAND gate or an inverter is 1 ns. Complete the timing diagram given in the figure, which shows the signal values with 1 ns resolution.



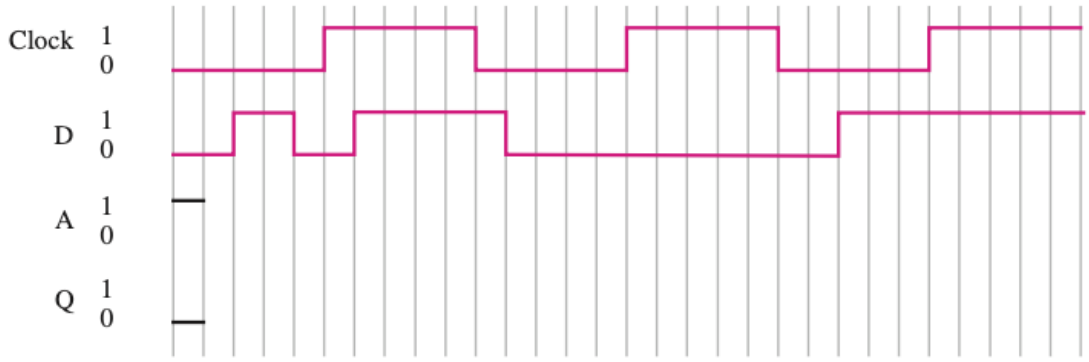


Figure P5.7 Circuit and timing diagram for Problem 5.25.