Homework 9: EE 252 Digital Electronics

1.- Show how a JK flip-flop can be constructed using a T flip-flop and other logic gates.

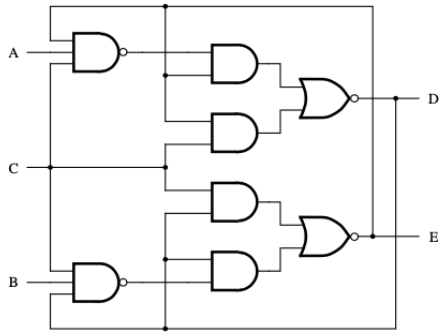
2.- Determine the counting sequence for the Verilog code below, starting with the pattern 010

```
module counter (R, L, Clock, Q);

        input [0:2] R;
        input L, Clock;
        output reg [0:2] Q;

        always @(posedge Clock)
                if (L)
                    Q < = R;
                else
                    Q < = {Q[2], Q[0]^Q[2], Q[1]};
endmodule
```

3. Consider the circuit in the figure below. Assume that the two NAND gates have about four times more propagation delay than the other gates in the circuit. How does the circuit compare with other circuits covered in class?



4.- Design a counter that counts pulses on line w and displays the count in the sequence 0,2,1,5,0,2,.... Use JK flip-flops in your circuit.