

EE 231 – Homework 4
Due September 24, 2010

1. Find all the prime implicants for the following Boolean functions, and determine which are essential. Then simplify the expressions.

(a) $F(w, x, y, z) = \Sigma(0, 1, 4, 5, 5, 7, 8, 9, 13, 15)$

		yz			
		00	01	11	10
$w x$	00	0	1	3	2
	01	4	5	7	6
	11	12	13	15	14
	10	8	9	11	10
		1	1	0	0
		1	1	1	1
		0	1	1	0
		1	1	0	0

Prime implicants: $w'y', w'x, xz, y'z, x'y'$
 Essential: $w'x$ (only one with 6), xz (only one with 15), $x'y'$ (only one with 8)
 Simplified: $w'x + xz + x'y' + w'y'$ or $w'x + xz + x'y' + w'x$

(b) $F(A, B, C, D) = \Sigma(0, 1, 2, 3, 6, 7, 8, 9, 13, 15)$

		CD			
		00	01	11	10
AB	00	0	1	3	2
	01	4	5	7	6
	11	12	13	15	14
	10	8	9	11	10
		1	1	1	1
		0	0	1	1
		0	1	1	0
		1	1	0	0

Prime implicants: $A'B', A'C, B'C', BCD, AC'D, ABD$
 Essential: $A'C$ (only one with 6), $B'C'$ (only one with 8)
 Simplified: $A'C + B'C' + ABD$

(c) $F(A, B, C, D) = \Sigma(0, 2, 3, 4, 6, 7, 9, 11, 13, 15)$

		<i>CD</i>			
		00	01	11	10
<i>AB</i>	00	0 1	1 0	3 1	2 1
	01	4 1	5 0	7 1	6 1
	11	12 0	13 1	15 1	14 0
	10	8 0	9 1	11 1	10 0

Prime implicants: $A'C, A'D', CD, AD$

Essential: $A'C'$ (only one with 0 and 4), AD (only one with 9 and 13)

Simplified: $A'C' + AD + CD$ or $A'C' + AD + A'C$

2. Find the minterms of the following Boolean expressions by first plotting each function in a map:

(a) $x'z' + y'z' + z'y'z'$

		<i>yz</i>			
		00	01	11	10
<i>x</i>	0	0 1	1 0	3 0	2 1
	1	4 1	5 0	7 0	6 1

$F(x, y, z) = \Sigma(0, 2, 4, 6)$

(b) $A'B + BC'D' + AC'D' + A'CD$

		<i>CD</i>			
		00	01	11	10
<i>AB</i>	00	0 0	1 0	3 1	2 0
	01	4 1	5 1	7 1	6 1
	11	12 1	13 0	15 0	14 0
	10	8 1	9 0	11 0	10 0

$F(A, B, C, D) = \Sigma(3, 4, 5, 6, 7, 8, 12)$

(c) $w'xy' + yz + xy'z'$

		<i>yz</i>			
		00	01	11	10
<i>wx</i>	00	0 0	1 0	3 1	2 0
	01	4 1	5 1	7 1	6 0
	11	12 1	13 0	15 1	14 0
	10	8 0	9 0	11 1	10 0

$F(w, x, y, z) = \Sigma(3, 4, 5, 7, 11, 12, 15)$

3. Simplify the following Boolean function using five-variable maps:

$F(A, B, C, D, E) = \Sigma(4, 5, 6, 7, 8, 9, 10, 11, 14, 19, 20, 21, 22, 23, 27, 30, 31)$

		<i>DE</i>			
		00	01	11	10
<i>BC</i>	00	0 0	1 0	3 0	2 0
	01	4 1	5 1	7 1	6 1
	11	12 0	13 0	15 0	14 1
	10	8 1	9 1	11 1	10 1

$A = 0$

		<i>DE</i>			
		00	01	11	10
<i>BC</i>	00	16 0	17 0	19 1	18 0
	01	20 1	21 1	23 1	22 1
	11	28 0	29 0	31 1	30 1
	10	24 0	25 0	27 1	26 0

$A = 1$

$F = B'C + A'BC' + ADE + CDE'$

4. Simplify the following Boolean function to product-of-sums form:

(a) $F(w, x, y, z) = \Sigma(0, 1, 4, 5, 6, 13)$

		<i>yz</i>			
		00	01	11	10
<i>wx</i>	00	0 1	1 1	3 0	2 0
	01	4 1	5 1	7 0	6 1
	11	12 0	13 1	15 0	14 0
	10	8 0	9 0	11 0	10 0

$F = (w' + x)(y' + z')(w' + z)(x + y')$

(b) $F(w, x, y, z) = \Pi(0, 2, 3, 5, 7, 8, 10, 11, 13, 15)$

		yz			
		00	01	11	10
$w x$	00	0 0	1 1	3 0	2 0
	01	4 1	5 0	7 0	6 1
	11	12 1	13 0	15 0	14 1
	10	8 0	9 1	11 0	10 0

$$F = (x' + z')(y' + z')(x + z)$$

5. Simplify the following Boolean function F , together with the don't-care conditions d .

(a) $F(x, y, z) = \Sigma(0, 1, 2, 3, 4, 6, 12)$
 $d(x, y, z) = \Sigma(5, 10, 11, 13)$

		yz			
		00	01	11	10
$w x$	00	0 1	1 1	3 1	2 1
	01	4 1	5 x	7 0	6 1
	11	12 1	13 x	15 0	14 0
	10	8 0	9 0	11 x	10 x

$$F = w'x' + w'z' + xy'$$

(b) $F(w, x, y, z) = \Sigma(4, 12, 13)$
 $d(w, x, y, z) = \Sigma(0, 1, 2, 6, 7, 9)$

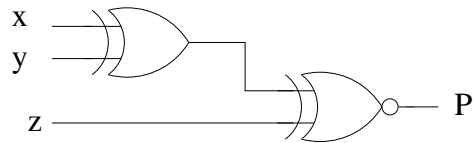
		yz			
		00	01	11	10
$w x$	00	0 x	1 x	3 0	2 x
	01	4 1	5 0	7 x	6 x
	11	12 1	13 1	15 0	14 0
	10	8 0	9 x	11 0	10 0

$$F = xy'z' + wy'z \text{ (and other ways)}$$

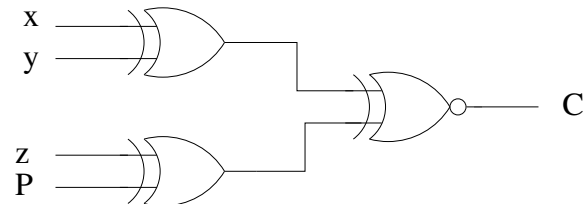
6. Problem 3.28

The 3-bit odd parity generator looks for an odd number of ones. It is just the 3-bit even circuit followed by an inverter, or the final gate is an XNOR rather than an XOR.

The 3-bit odd parity checker looks for an odd number of ones. It is just the 3-bit even circuit followed by an inverter, or the final gate is an XNOR rather than an XOR.



(a) 3-bit odd parity generator



(b) 4-bit odd parity checker

7. Write a Verilog gate-level description of the circuit shown in

(a) Fig. 4.2 (p. 124)

```

module p7a(input A, B, C, output F1, F2);

  wire T1,T2,T3,w4,w5,w6,w7;

  AND (T2,A,B,C);
  OR  (T1,A,B,C);
  AND (w4,A,B);
  AND (w5,A,C);
  AND (w6,B,C);
  OR  (F2,w4,w5,w6);
  AND (T3,T1,~F2);
  OR  (F1,T2,T3);

endmodule

```

(b) Fig. 4.4 (p.129)

```

module p7b(input A, B, C, D, output w, x, y, z);

    wire CandD,CorD,w1,w2,w3);

    AND (CandD,C,D);
    OR  (CorD,D,D);
    NOT (z,D);
    OR  (y,CandD,~CorD);
    AND (w1,(~CorD,B);
    AND (w2,CorD,~B);
    AND (w3,CorD,B);
    OR  (x,w1,w2);
    OR  (w,w3,A);

    endmodule

```

8. Using continuous assignment statements, write a Verilog description of the circuit shown in

(a) Fig. 4.2 (p. 124)

```

module p8a(input A, B, C, output F1, F2);
    /* From the equations for F1 and F2 on Page 125 */

    assign F2 = A&B | A&C | B&C;
    assign F1 = ~A&B&~C | ~A&~B&C | A&~B&~C | A&B&C;

    endmodule

```

(b) Fig. 4.4 (p.129)

```

module p8b(input A, B, C, D, output w, x, y, z);
    /* From the equations on Page 129 */

    assign z = ~D;
    assign y = C&D | ~C&~D;
    assign x = ~B&C | ~B&D | B&~C&~D;
    assign w = A | B&C | B&D;

    endmodule

```