EE 231 – Homework 5
Due October 1, 2010

1. For the circuit shown in Fig. 4.26 (page 155 of the text),
   (a) Write the Boolean function for the outputs in terms of the input variables.
   (b) If the circuit is listed in a truth table, how many rows would there be in the table?
   (c) Write a Verilog dataflow model for the circuit.

2. A majority circuit is a circuit with an odd number of inputs whose output is a 1 if and only if a majority of its inputs are 1.
   (a) Find the truth table for a three-input majority circuit.
   (b) From the truth table, find the Boolean equation for the circuit.
   (c) Write a Verilog dataflow model of the circuit.

3. Problem 4.8. Treat this as a 4-input, 4-output combinational circuit, find the truth table, and use Karnaugh maps to simplify.

4. (a) Design a full subtractor circuit with three inputs x, y, B_{in}, and two outputs D and B_{out}. The circuit subtracts $x - y - B_{in}$. B_{out} is 0 if no borroow is needed to complete the subtraction, and 1 if a borrow is needed. Find the truth table, and simplify the equations for D and B_{out} using Karnaugh maps.
   (b) Draw a block diagram showing how four full subtractors can be used to implement a 4-bit subtraction.
   (c) Write a Verilog dataflow model to implement the circuit of Part (b).

5. (a) The adder-subtractor circuit of Fig. 4.13 has the following values for mode input M and data inputs A and B:

	M	A	B
(a)	0	0011	0101
(b)	0	1101	1101
(c)	1	0100	0011
(d)	1	0000	0001

   In each case determine the values of the four SUM outputs, the carry C, and overflow V.
   (b) Using the conditional operator (?:), write a Verilog dataflow description of the four-bit adder-subtractor of Fig. 4.13.

6. For the circuit shown in Fig. 4.13 of the text, verify that the V output bit is correct for the addition operation. That is, show that (a) V will be 1 when you add two positive numbers together ($B_3 = 0$ and $A_3 = 0$) and get a negative number ($S_3 = 1$), (b) V will be 1 when you add two negative numbers together ($B_3 = 1$ and $A_3 = 1$) and you get a positive number ($S_3 = 0$), and (c) the V output will be 0 in all other circumstances (adding two positives and getting a positive, adding two negatives and getting a negative, or adding a positive and a negative number).

7. Assume that inverter gates have a propagation delay of 5 ns and that AND, OR, NAND and NOR gates have a propagation delay of 10 ns. What is the total propagation delay of the four-bit magnitude comparator circuit of Fig. 4.17?