EE 231 – Homework 6
Due October 8, 2010

1. Problem 4.16

2. Using a decoder and external gates, design the combinational circuit defined by the following three Boolean functions:

   (a) $F_1 = x'y'z + xz'$
   $F_2 = x'yz' + xy'$
   $F_3 = xyz' + xy$

   (b) $F_1 = (x + y')z'$
   $F_2 = xz + y'z + yz'$
   $F_3 = (y + z')x$

3. Implement the following Boolean functions with a multiplexer:

   (a) $F(w, x, y, z) = \Sigma(2, 3, 5, 6, 11, 14, 15)$

   (b) $F(w, x, y, z) = \Pi(3, 10, 11)$

4. Write a Verilog dataflow description to implement the Boolean functions of Problem 3.

5. Implement a full adder with two 4x1 multiplexers. Note: the truth table for the full subtractor is:

x	y	C_{in}	C_{out}	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	1	0
1	1	1	1	1

6. An 8x1 multiplexer has inputs A, B and C connected to the selection inputs S_2, S_1, and S_0 respectively. The data inputs through I_0 through I_7 are as follows:

   (a) $I_1 = I_2 = I_4 = 0; I_3 = I_5 = 1; I_0 = I_7 = D$; and $I_6 = D'$.

   (b) $I_2 = I_3 = 0; I_4 = I_5 = I_7 = 1; I_0 = I_6 = D$; and $I_1 = D'$.

   Determine the Boolean function that the multiplexer implements.

7. Problem 4.39. Use a behavioral description to implement the problem. Do not write a gate level or dataflow description.

8. Problem 4.50.

9. Using a case statement, write an HDL behavioral description of an eight-bit arithmetic-logic unit (ALU). The ALU needs to implement the 10 functions listed below. The inputs are two eight-bit numbers A and B, and select inputs S (where S has enough bits to select the ten functions). The outputs are the eight-bit result R, a zero-bit Z, and a carry bit C. The C bit is described in the table below. (X means Don't Care.) The zero bit Z is 1 if all the bits of the eight-bit result are 0, and is 0 otherwise.

Name	Description	R	C	Z
LOAD	Load input A	A	X	1 if $R == 0$
ADDA	Add inputs	$A + B$	Carry	1 if $R == 0$
SUBA	Subtract inputs	$A - B$	Borrow	1 if $R == 0$
ANDA	AND inputs	$A\&B$	X	1 if $R == 0$
ORAA	OR inputs	$A\|B$	X	1 if $R == 0$
COMA	Bitwise Complement input A	$\sim A$	1	1 if $R == 0$
INCA	Increment input A	$A + 1$	X	1 if $R == 0$
LSRA	Logical Shift Right input A	$0 => R[7]$ $A[7:1] => R[6:0]$	$A[0]$	1 if $R == 0$
LSLA	Logical Shift Left input A	$0 => R[0]$ $A[6:0] => R[7:1]$	$A[7]$	1 if $R == 0$
ASRA	Arithmetic Shift Right input A	$A[7] => R[7]$ $A[7:1] => R[6:0]$	$A[0]$	1 if $R == 0$