EE 231

Homework 9

Due October 29, 2010

1. A serial parity-bit generator is a sequential circuit that does the following: it receives an n-bit message followed by a 0 (so there are $n + 1$ clock bits to send the message). At the output, the circuit sends the original n-bit message, but replaces the 0 with a parity bit. Design a 4-bit serial parity-bit generator which replaces the zero bit with an odd parity bit.

   (a) Draw a state diagram for the circuit.

   (b) Draw a state transition table for the circuit.

   (c) Show how to implement the circuit using D flip-flops.

   (d) Write a Verilog program to implement the circuit.

   (e) Is this a Mealy machine or a Moore machine? Why?

2. Design a synchronous sequential circuit that will count through the sequence 0, 2, 4, 6 when its control input x is 0, and through the sequence 6, 4, 2, 0 when $x = 1$. The circuit should return to the 0 state if it finds itself in an invalid state.

   (a) Draw a state diagram for the circuit.

   (b) Draw a state transition table for the circuit.

   (c) Write a Verilog module to implement the system.

3. The serial adder of Fig. 6.6 uses two four-bit shift registers. Register A holds the binary number 1101 and register B holds 0110. The carry flip-flop is initially reset to 0. List the binary values in register A and the carry flip-flop after each shift.

4. Consider the following Verilog statements

   (a)
   ```
   RegA <= 32;
   RegB <= RegA;
   ```
   Assume that `RegA` contains the value of 45 and `RegB` contains the value of 32 initially. What are the values of `RegA` and `RegB` after execution?

   (b)
   ```
   RegA = 32;
   RegB = RegA;
   ```
   Assume that `RegA` contains the value of 45 and `RegB` contains the value of 32 initially. What are the values of `RegA` and `RegB` after execution?

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5. Consider the following Verilog code fragment:

```
reg [3:0] A, B;

always @( posedge clock )
begin
A = 5;
B = A + 2;
end
```

   Before the clock edge, `A` has the value of 3, and `B` has the value of 6. What will be the values of `A` and `B` after the clock edge?

6. Consider the following Verilog code fragment:

```
reg [3:0] A, B;

always @( posedge clock )
begin
A <= 5;
B <= A + 2;
end
```

   Before the clock edge, `A` has the value of 3, and `B` has the value of 6. What will be the values of `A` and `B` after the clock edge?