EE 231

Homework 11

Due November 15, 2010

1. The memory units that follow are specified by the number of words times the number of bits per word. How many address lines and input-output data lines are needed in each case?

   (a) 32 x 8

   (b) 4M x 16

   (c) 2G x 32

2. Give the number of bytes stored in the memories listed in Problem 1.

3. A DRAM chip uses two-dimensional address demultiplexing. It has 16 common address pins, with the row address having four more bits than the column address (the row address has 16 bits, the column address has 12 bits). What is the capacity of the memory?

4. This problem deals with the Hamming code for error detection and correction. To be able to detect and correct one-bit errors for eight-bit words, five parity bits are required. The numbers are of the form P_0 P_1 P_2 D_3 P_4 D_5 D_6 D_7 P_8 D_9 D_{10} D_{11} D_{12}, where P_0 is the overall parity bit (called P_{13} in the text), and D_3 D_5 D_6 D_7 D_9 D_{10} D_{11} D_{12} is the original 8-bit data word.

   (a) You read the number 0001 0101 1000 0 from a memory which uses error detection and correction. What was the original 8-bit data word that was written?

   (b) Repeat (a) for the number 1010 0001 0110 0.

   (c) Repeat (a) for the number 1110 0111 1100 1.

5. This problem deals with the Hamming code for error detection and correction. To be able to detect and correct one-bit errors for eight-bit words, five parity bits are required.

   (a) What is the code to store the number 1001 0110

   (b) Repeat (a) for the number 1011 1101

   (c) Repeat (a) for the number 0100 1011