EE 231

Homework 13

Due December 3, 2010

1. Explain in words and write the HDL statements for the operations specified by the following register transfer notations;

   (a) $R1 \leftarrow R1 - 1, R2 \leftarrow R1$

   (b) $R3 \leftarrow shr\ R3$

   (c) If $(S = 0)$ then $(R0 \leftarrow shr\ R0)$ else $(R0 \leftarrow shl\ R0)$

2. Construct a block diagram and an ASMD chart, and write a Verilog program, which controls a machine which dispenses a can of soda. The machine will accept pennies, nickels, dimes and quarters. Only one coin will go through the machine at a time, and that coin will be detected for exactly one clock cycle. The dispense output should go high for one clock cycle when the total amount of money inserted is equal to or greater than 60 cents. If the total is greater than 60 cents, the excess is held in the register to be used for the next soda. For example, if 75 cents is deposited, the machine should dispense a soda, and leave 15 cents towards the next soda.

   The datapath should consist of a register to hold the total amount, a combinational circuit which can add the amount deposited to the register and subtract the cost of the soda from the register, and a display showing how much money is available for the soda.

   The controller should have a reset input to reset the count to zero.

3. Design a reaction timer system, which measures the amount of time elapsed between turning on a light and the user pressing a button. The system has three inputs: a 1 kHz clock, a reset button, and the user button B. It has three outputs: a one-bit output L to turn on an LED, a 12-bit output T to display the reaction time, and a one-bit output S which is activated if the user is too slow. After the reset button is pushed, the system waits for 10 seconds, then activates the L output, and starts counting on the T register. When the user presses the B button, the T value is held. If the user is too slow, and fails to press the button within 2 seconds, the S output is activated, and the T register displays 2,000.

   Construct a block diagram (controller and datapath) and an ASMD chart, and write a Verilog program, to implement the reaction timer.