EE 231 – Homework 4
Due September 25, 2009

1. Find all the prime implicants for the following Boolean functions, and determine which are essential. Then simplify the expressions.

   (a) $F(w, x, y, z) = \Sigma(0, 1, 2, 3, 5, 7, 8, 10, 12, 13)$

   (b) $F(A, B, C, D) = \Sigma(0, 1, 4, 5, 6, 7, 9, 11, 14, 15)$

   (c) $F(A, B, C, D) = \Sigma(1, 3, 5, 7, 8, 10, 11, 12, 14, 15)$

2. Find the minterms of the following Boolean expressions by first plotting each function in a map:

   (a) $x'y' + y'z' + x'yz'$

   (b) $CD' + A'B'C + A'B'D + ABD'$

   (c) $w'y'z' + wx + w'x'z$

3. Simplify the following Boolean function using five-variable maps:

   $F(A, B, C, D, E) = \Sigma(0, 1, 5, 9, 13, 16, 17, 20, 21)$

4. Simplify the following Boolean function to product-of-sums form:

   (a) $F(w, x, y, z) = \Sigma(1, 8, 9, 10, 12, 13)$

   (b) $F(w, x, y, z) = \Pi(0, 2, 4, 6, 9, 11, 13, 15)$

5. Simplify the following Boolean function F, together with the don't-care conditions d.

   (a) $F(x, y, z) = \Sigma(0, 2, 3, 6, 7)$
       $d(x, y, z) = \Sigma(1, 4, 5)$

   (b) $F(w, x, y, z) = \Sigma(1, 3, 8, 10, 15)$
       $d(w, x, y, z) = \Pi(2, 4, 9, 11)$

6. Problem 3.28

7. Write a Verilog gate-leve description of the circuit shown in

   (a) Fig. 3.36(a)

   (b) Fig. 3.36(b)

8. Using continuous assignment statements, write a Verilog description of the circuit shown in

   (a) Fig. 3.36(a)

   (b) Fig. 3.36(b)