EE 231 – Homework 7
Due October 16, 2009

1. Problem 5.1
2. Problem 5.4
3. A sequential circuit with two D flip-flops A and B, two inputs x and y, and one output z is specified by the following next-state and output equations:

$$\begin{aligned} A(t+1) &= xy' + xB \\ B(t+1) &= y'A + xB \\ z &= A \end{aligned}$$

   (a) Draw the logic diagram of the circuit.

   (b) List the state table for the circuit.

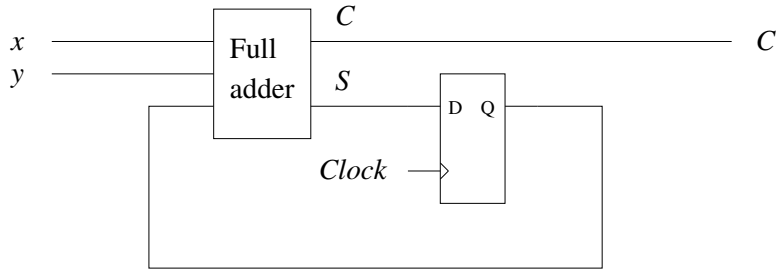
   (c) Draw the corresponding state diagram.

4. A sequential circuit has one flip-flip Q, two inputs x and y, and one output C. It consists of a full adder circuit connected to a D flip-flop, as shown below.

   (a) Derive the state table of the sequential circuit.

   (b) Derive the state diagram of the sequential circuit.

   (c) Write a Verilog module to implement the circuit.



5. Derive the state table and state diagram of the sequential circuit shown below. Explain the function that the circuit performs.