EE 231

Homework 9

Due October 28, 2009

1. Design a sequential circuit with two flip-flops A and B and one input x_in. When $x\_in = 0$, the state of the circuit remains the same. When $x\_in = 1$, the circuit goes through the state transitions from 00 to 10, to 11, to 01, back to 00, then repeats. The sytem should have an active low asynchronous reset which resets the system to 00.

   (a) Draw a state diagram for the system.

   (b) Make a state transition table for the system.

   (c) Find the equations for the inputs to the D flip-flops, and draw a circuit for the system.

   (d) Write a Verilog module to implement the system.

2. Design a one-input, one-output serial 2's complementer. The circuit accepts a string of bits from the input and generates the 2's complement at the output. The circuit can be reset asynchronously to start and end the operation. The bits come in least-significant bit first. (Hint: This function can be implemented with only two states, so requires only one flip-flop. From Page 11 of the text: "The 2's complement can be formed by leaving all least significant 0's and the first 1 unchanged, and replacing 1's with 0's and 0's with 1's in all other higher significant digits.")

   (a) Draw a state diagram for the system.

   (b) Make a state transition table for the system.

   (c) Find the equation for the input to the D flip-flop, and draw a logic diagram to implement the function.

   (d) Write a Verilog module to implement the system.

   (e) Is this a Mealy machine or a Moore machine?

3. Problem 5.19 (a).

   (a) Make a state transition table for the system.

   (b) Find the equations for the inputs to the D flip-flops. You do not have to draw the logic diagram.

   (c) Write a Verilog module to implement the system.

   (d) Is this a Mealy machine or a Moore machine?

4. Consider the following statements, assuming that `RegA` contains the value of 27 and `RegB` contains the value of 35 initially:

   (a)
   ```
   RegA = 53;
   RegB = RegA;
   ```

   (b)
   ```
   RegA <= 53;
   RegB <= RegA;
   ```

   What are the values of `RegA` and `RegB` after execution?