EE 231

Homework 10

Due November 4, 2009

1. Design a four-bit shift register with parallel load using D flip-flops. There are two control inputs: *shift* and *load*. When *shift* = 1, the contents of the register are shifted one position to the right. New data are loaded if *load* = 1 and *shift* = 0. If both the control inputs are 0, the contents of the register do not change.

2. Show how to connect four 4-bit binary counters of the type of Figure 6.14 to make a 16-bit binary counter.

3. Design a three-bit sequential circuit controlled by the input w. If $w = 1$, the counter adds 2 to its contents, wrapping around if the count reaches 6 or 7. (If the present state is 6 or 7, the next state becomes 0 or 1 respectively.) If $w = 0$, the counter subtracts 1 from its contents, acting as a normal down-counter.

   (a) Draw the state diagram for the system.

   (b) Make the state transition table for the system.

   (c) Find the excitation equations for the system (the equations for the inputs to each of the D flip-flops).

   (d) Write a Verilog program to implement the system.

4. Design a sequential system with one input x, one output z, and a clock. The system will detect the occurence of the sequence 0101 on the input x. When it observes the pattern 0101, the output z will go high for one clock cycle, then go low again until it sees the pattern again. The output z will go high even if the sequences overlap. Here is an example:

   x: `010001010100101`
   z: `000000010100001`

   (a) Draw the state diagram for the system.

   (b) Make the state transition table for the system.

   (c) Find the excitation equations for the system (the equations for the inputs to each of the D flip-flops).

   (d) Write a Verilog program to implement the system.