EE 231

Homework 12

Due November 20, 2009

1. The memory units that follow are specified by the number of words times the number of bits per word. How many address lines and input-output data lines are needed in each case?

   (a) 16K x 8

   (b) 2M x 16

   (c) 4G x 32

2. Give the number of bytes stored in the memories listed in Problem 1.

3. A DRAM chip uses two-dimensional address demultiplexing. It has 14 common address pins, with the row address having two more bits than the column address. What is the capacity of the memory?

4. This problem deals with the Hamming code for error detection and correction. The numbers are of the form $P_0\ P_1\ P_2\ D_3\ P_4\ D_5\ D_6\ D_7\ P_8\ D_9\ D_{10}\ D_{11}\ D_{12}$, where P_0 is the overall parity bit (called P_{13} in the text).

   (a) You read the number 1011 0110 0100 1 from a memory which uses error detection and correction. What was the original 8-bit data word that was written?

   (b) Repeat (a) for the number 1011 1101 0001 1.

   (c) Repeat (a) for the number 1000 1011 1100 1.

5. A ROM chip of 8,192 x 16 bits has two chip select inputs and operates from a 5-volt power supply. How many pins are needed for the integrated circuit? Draw a block diagram and label all input and output terminals in the ROM.

6. Problem 7.17

7. Specify the size of a ROM (number of words and number of bits per word) that will accomodate the truth table for the following combinational circuit components:

   (a) a binary multiplier the muliplies two 8-bit binary words.

   (b) a double four-to-one line multiplexer with common select and enable inputs

   (c) a BCD-to-seven segment decoder with an enable input

8. Derive the PAL programming table to the BCD-to-excess-3-code converter whose Boolean functions are simplified in Figure 4.23 of the text. Draw the corresponding fuses on the attached PAL figure.

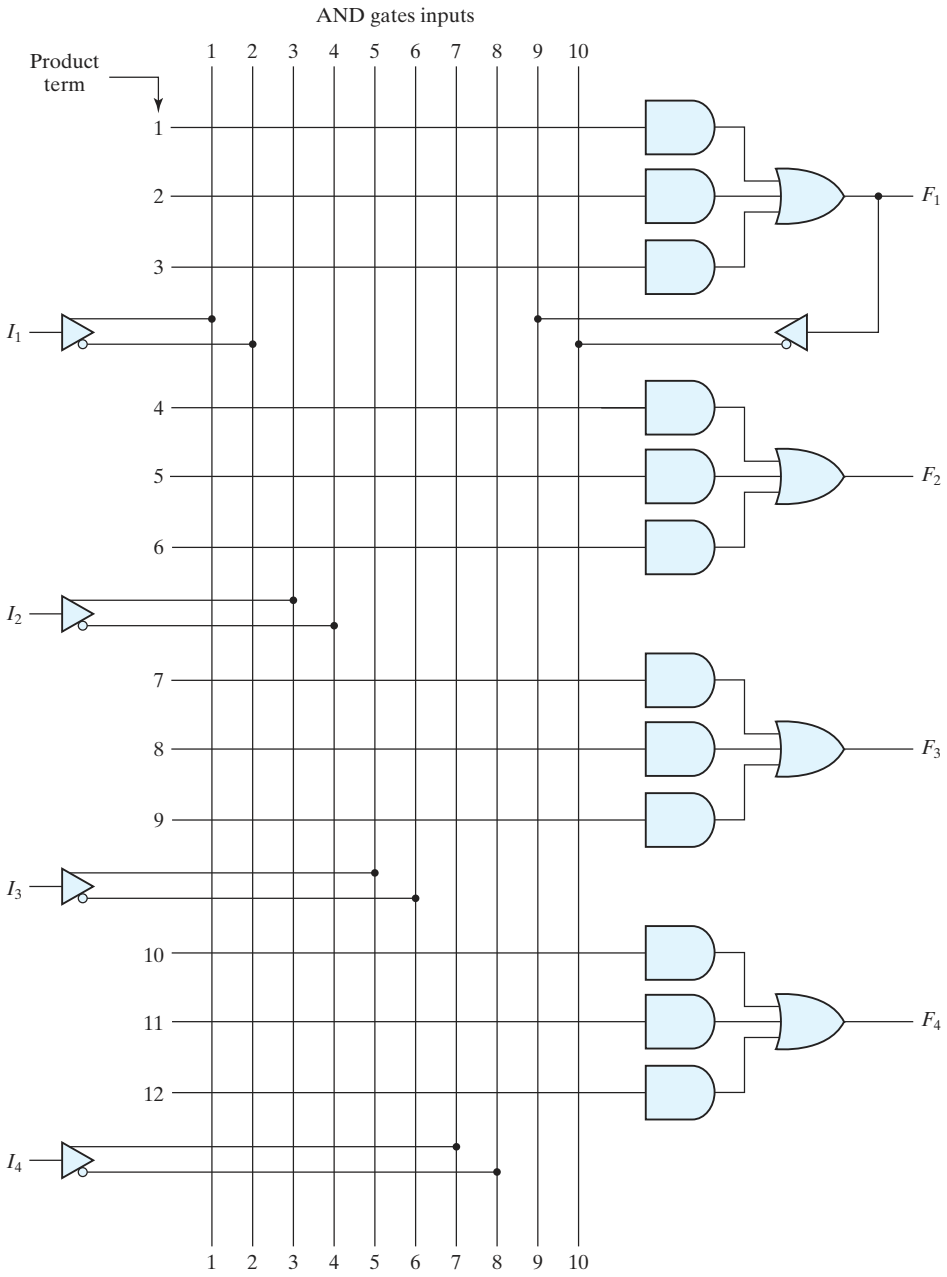

Figure Number: 07 16
Mano/Ciletti
Digital Design, 4e