EE 231

Exam 4

December 8, 2008

Name: _____

Show all work. Partial credit will be given. No credit will be given if an answer appears with no supporting work.

1. How many address and data lines are needed for the following memory units? How many bytes of memory does each unit hold?

   (a) 256M x 16

   (b) 4K x 32

2. The following two problems deal with the Hamming code for error detection and correction. For (a) and (b), the numbers are of the form $P_0\ P_1\ P_2\ D_3\ P_4\ D_5\ D_6\ D_7\ P_8\ D_9\ D_{10}\ D_{11}\ D_{12}$, where P_0 is the overall parity bit.

   (a) Consider the binary number 01011010_2. Generate the Hamming code for the number which will allow you to correct one-bit errors and detect two-bit errors.

   (b) You read the number $0\ 1011\ 0010\ 1110$ from a memory which uses error detection and correction. What was the original 8-bit data word which was written to memory?

   (c) How many bits are needed to correct one-bit errors and detect two-bit errors for a 24-bit data word? Explain.

3. Assume that $A = 4'b1011$, $B = 4'b1101$ and $C = 4'b0000$. Show the results of the following Verilog operations:

   (a) `A + B` _____

   (b) `A - B` _____

   (c) `A & B` _____

   (d) `A && B` _____

   (e) `A | C` _____

   (f) `A || C` _____

   (g) `A >> 2` _____

   (h) `A >>> 2` _____

4. Show the PAL fuse map for implementing the following functions. Be sure to explain your work.

   $A(w, x, y, z) = \sum(4, 5, 10, 11, 12, 13, 14, 15)$
   $B(w, x, y, z) = \sum(6, 7, 8, 9, 12, 13, 14, 15)$
   $C(w, x, y, z) = \sum(0, 2, 7, 8, 9, 10, 12, 13, 14, 15)$

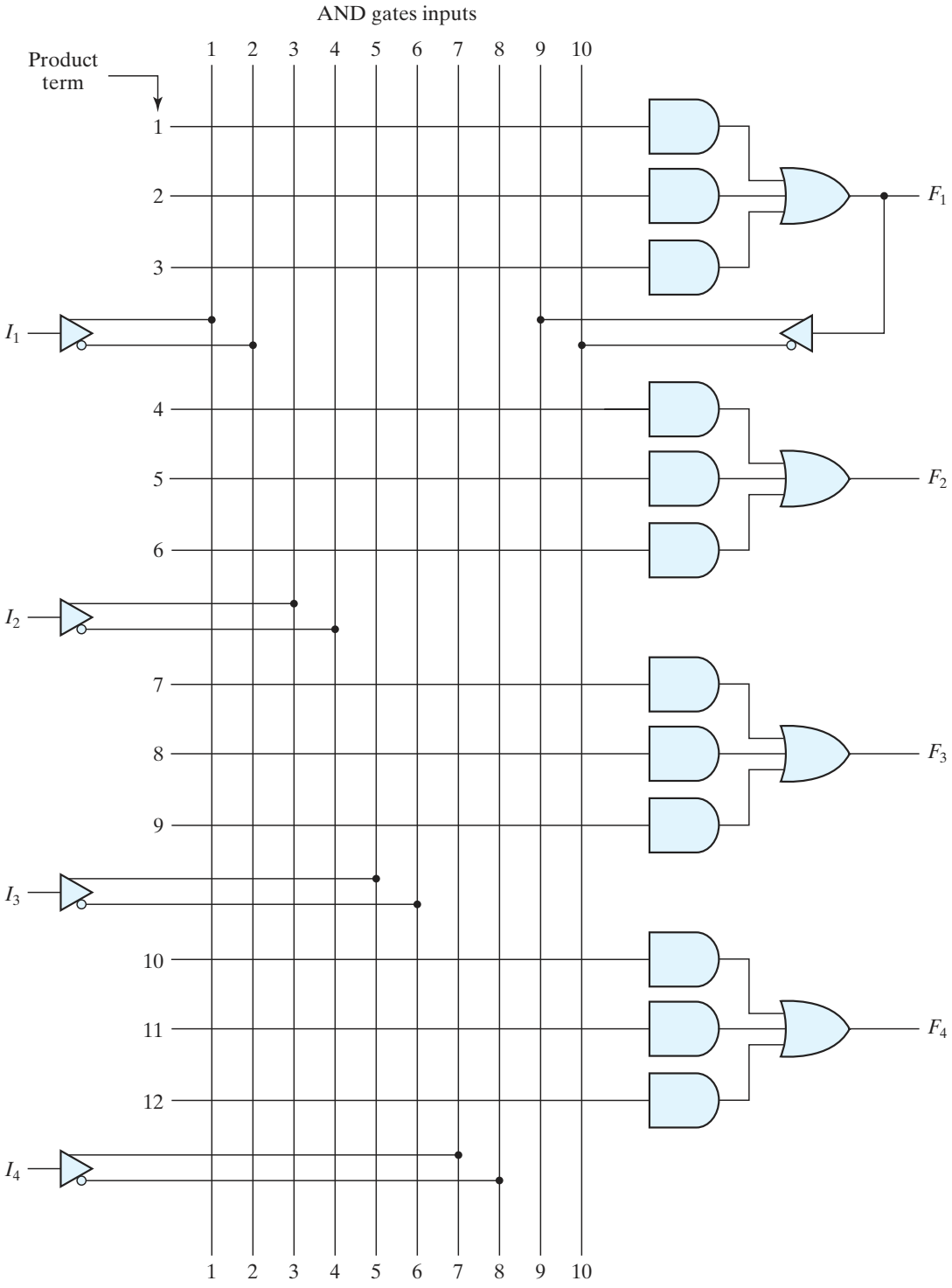

Figure Number: 07 16
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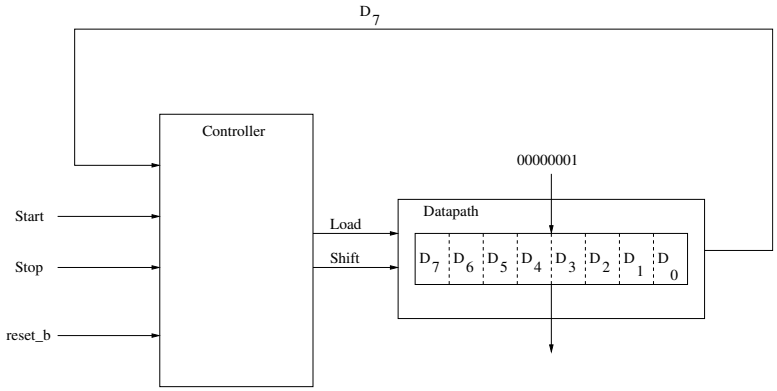
Digital Design, 4e

5. The figure below shows the controller and the datapath for a digital circuit. The `Load` signal loads 0000001 into Register D. The `Shift` signal shifts Register D left by 1. The circuit is supposed to do the following: `reset_b` is an asynchronous reset, which puts the system into the `S_idle` state. The system remains in the `S_idle` state until the controller sees the `Start` signal go high. When `Start` goes high, the system loads the 00000001 into Register D and goes to the `S_running` state. After that, the system shifts Register D left until the 1 is in bit D_7, at which point the system will reload D with 00000001. It will continue doing this until `Stop` goes high. When `Stop` goes high, the system returns to the `S_idle` state. The system will generate the following pattern, a ring counter in which a single 1 rotates through the bits:

   00000001, 00000010, 00000100, 00001000, 00010000, 00100000, 01000000, 10000000, 00000001, 00000010,

   Draw an ASMD chart for this circuit.



6. Consider the following ASMD chart. Draw the state transition diagram for the controller.