EE 231 – Homework 7 Due October 15, 2010

- 1. Show how to build a J-K flip-flop using a T flip-flop and some combinational logic.
- 2. Figure 5.6 of the text shows one way to build a D latch. The figure below shows another way. Show that the below functions identically to the D latch of Figure 5.6.



3. A sequential circuit with two D flip-flops A and B, one input x, and one output z is specified by the following next-state and output equations:

$$A(t+1) = A' + B$$

$$B(t+1) = B'x$$

$$z = A + B'$$

- (a) Draw the logic diagram of the circuit.
- (b) List the state table for the circuit.
- (c) Draw the corresponding state diagram.

- 4. A sequential circuit has three flip-flips A, B and C, and two inputs x and y, as shown below.
 - (a) Derive the state table of the sequential circuit.
 - (b) Derive the state diagram of the sequential circuit.
 - (c) Write a Verilog module to implement the circuit.



5. Derive the state table and state diagram of the sequential circuit shown below. Draw a timing diagram for clk, x, A and B for 10 clock ticks, assuming that the machine starts in state 00 and x is always 1. Explain the function that the circuit performs.

