EE 231L

Getting Started with MAX+plus II

MAX+plus II is a software package from Altera which you will use to compile and simulate your PLD designs. Here is a brief tutorial for using MAX+plus II. For a more detailed tutorial, look in the *MAX+PLUS II Getting Started Manual*, which is available on the Altera website.

1. Find the MAX+plus II program. It should be a button in the lower-left corner of the screen next to the Start menu. Open the Max+plus II program.

2. From the **File** menu choose **Project** and choose **Name**. (Or click on the  button on the menu bar.) Change to the subdirectory for this lab, or make a subdirectory for this lab if you haven't already done so. (Altera generates multiple files for each project. Having an organized file system will be VERY helpful when combining the separate elements of the final computer for EE 231 lab).

3. Enter a name such as Majority. This name will be given to the many files created by the program, and should also be the name of your SUBDESIGN.

4. From the **File** menu choose **New** (or click on the  button on the menu bar.) , select the file type you wish to enter your circuit with (TDF files are entered using the Text Editor, GDF files are entered with the Graphic Editor). Click OK. Now choose **File**, **Save As**, and save with the same name as the project name. Enter the program. Choose **File**, **Project**, **Save and Check** (or click on the  button on the menu bar). After it saves with no errors, choose **Assign Device** from the **Assign** menu. Make sure Device Family is set to Max7000s and the Show only Fastest Speed Grade is not checked. Select the exact name written on your Altera chip from the list of chips given and click OK. Now click the **Start** button on the compiler window (or on the  button on the menu bar). After this compiles with no errors, you can check the design via a simulation.

5. To simulate and verify the program, first get a waveform window. Choose **New** from the **File** menu, select **Waveform Editor File** and .scf extension. Then choose **File**, **Save As**, and save with the same name as the project name (with an .scf extension). Choose **Enter Node Names from SNF** (**Node** menu). In the dialog box, under **Type**, **Inputs** and **Outputs** should be checked. Click the **List** button. Highlight the variables you want to view on the simulation and move them to the **Select** box with (=¿) button. Click **OK**. Chose **End Time** from the **File** menu, and increase the end time to 16us. You now should have a diagram with inputs and outputs versus time. The inputs are all 0, and the outputs are not determined. Click the small magnifying glass (tool bar in the left side of the screen) several times to zoom out to the full picture.

6. There are two ways to enter simulation waveforms. You can draw the input waveform with the mouse, or you can use the **Edit** menu. For example, for the majority circuit with inputs

called A, B,C: To make the A input high for the second half of the time, set the cursor on A near the center (8 us), press and hold the left mouse button, drag the cursor to the end (16 us) and release. Then click on the 1 menu option in the left-hand menu. A quick way to get alternating highs and lows on C is as follows. First, click on the **Option** menu. If there is a check mark by the **Snap to Grid** option, click on it to remove the check mark. Next, click and highlight all of C by clicking in the **Name** column. Next from the **Edit** menu choose **Overwrite** and **Count Value**. (You can also reach this menu by right-clicking on C in the **Name** column. Change the **Count Every** option to 1 us and click on OK. (If **Snap to Grid** is checked, you will not be allowed to choose the **Count Every** option.) Repeat for input B, changing the **Count Every** option to 2 us. Save this file.

7. Choose **Simulator** from the MAX+plusII menu, and **Start** it (or click on the  button on the menu bar).

8. Now you should have a simulated output. Verify that the output is what you expected.