EE 231L Lab 4

Prelab Part 2

The writeup for Lab 4 gives a code fragment for the state machine for the control system for a computer. It shows what should be on the output lines of the control system for two instructions: `LDAA addr` and `LDAA #num`. Make a table which shows what should which control lines should be active (`READ`, `STORE`, `INST_L`, `C_L`, `ACCA_L`, `PC_L`, `PC_I`, and `MAR_L`), and what should be on the `ALU_CTL` and `MEM_SEL` lines for the other instructions of the computer. Here is the start for the `LDAA addr` and `LDAA #num` instructions:

Instruction	State C1	State C2	State C3

`LDAA addr`	`INST_L, READ, PC_I`
	`PC` → `MEM_SEL`
	
	Next state: C2
		`MAR_L, READ, PC_I`
		`PC` → `MEM_SEL`
		
		Next State: C3
			`READ, ACCA_L`
			`MAR` → `MEM_SEL`
			`ALU_LOAD` → `ALU_CTL`
			Next State: C1

`LDAA #num`	`INST_L, READ, PC_I`
	`PC` → `MEM_SEL`
	
	Next state: C2
		`ACCA_L, READ, PC_I`
		`PC` → `MEM_SEL`
		`ALU_LOAD` → `ALU_CTL`
		Next State: C1	

`ADDA addr`	`INST_L, READ, PC_I`
	`PC` → `MEM_SEL`
	
	Next state: C2
		`MAR_L, READ, PC_I`
		`PC` → `MEM_SEL`
		
		Next State: C3
			`READ, ACCA_L`
			`MAR` → `MEM_SEL`
			`ALU_ADD` → `ALU_CTL`
			Next State: C1

Here are a few hints for finishing the table:

- The instructions `SUBA addr`, `ANDA addr`, `ORAA addr`, and `CMPA addr` are the same as `LDAA addr`, except for the `ALU_CTL` lines in State C3.
- The instructions `JMP addr` is similar to `LDAA addr`, except that in State C3, you need to load the data out of the memory chip into the `PC` register rather than into the `ACCA` register.