EE 231L Lab 5

Building the Computer

Now that you have designed and simulated your computer, it is time to build and test it. You will build the computer on a printed circuit board which has a socket for an Altera EPF8636ALC84 PLD and a Cypress CY7C128 memory chip. The EPF8636 in programmed in the circuit — you will not remove the chip and program it at the programming station. (The program in the EPF8636 is stored in volatile memory, so the program is lost when power is removed.) The printed circuit board has the hardware needed to program the EPF8636 through the parallel port on your lab computer. Figure 1 shows a diagram of the printed circuit board.

Figure 2 shows the first page of the data sheet for the memory chip you will use. Note that the memory chip has eleven address lines, while your design has only eight address lines. You should connect the three unused address lines (A10, A9, and A8) to VCC or ground. You then need to connect the eight address lines used by the computer (A7-A0), the eight data lines (called I/O 7-0 on the data sheet) and the three control lines — chip select (called $\overline{\text{CE}}$ on the data sheet), output enable, and write (called $\overline{\text{WE}}$ on the data sheet). (VCC and GND are already connected on the printed circuit board.)

It will be useful to assign pins on your EPF8636 in order to make the computer easier to build. Figure 3 shows the computer I built. I assigned Pin 43 to be the Output Enable line, Pin 44 to be the Write Enable line, Pin 46 to be Data 7, etc. I assigned the pins so that it would be convenient to wire the EPF8636 to the memory chip. I also assigned pins of the input port so they would be together, and I could connect the eight input lines to the source of the inputs. To assign pins in Max+Plus II, you go to the **Assign** menu, the **Pin/Location/Chip** sub-menu, and make the pin assignments there.

When you wire your computer, some of the pins on the EPF8636 are labeled V, G and P. The pins labeled V have been connected to +5V. Those labeled G have been connected to ground. Those labeled P are used for programming the EPF8636. Do not connect anything to the pins labeled P. You can use the pins labeled V or G to connect to the unused address lines of the memory chip. You should also connect a G pin on the printed circuit board to the ground on your breadboard. (You will use your breadboard to supply the clock for the computer, and input data.)

CY7C128A

2K x 8 Static RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 15 ns**
- **Low active power**
  - **— 660 mW (commercial)**
  - **— 688 mW (military—20 ns)**
- **Low standby power**
  - **— 110 mW (20 ns)**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **V_{IH} of 2.2V**

Functional Description

The CY7C128A is a high-performance CMOS static RAM organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), and active LOW Output Enable ($\overline{OE}$) and three-state drivers. The CY7C128A has an automatic power-down feature, reducing the power consumption by 83% when deselected.

Writing to the device is accomplished when the Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs are both LOW.

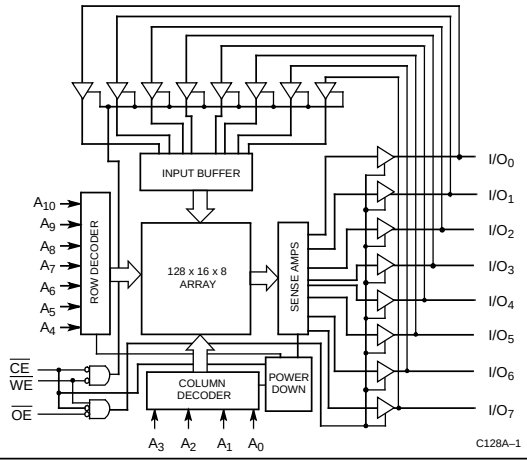
Data on the eight I/O pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{10}).

Reading the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while Write Enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight I/O pins.

The I/O pins remain in high-impedance state when Chip Enable ($\overline{CE}$) or Output Enable ($\overline{OE}$) is HIGH or Write Enable ($\overline{WE}$) is LOW.

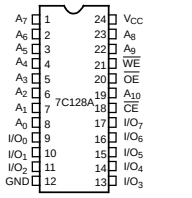
The CY7C128A utilizes a die coat to insure alpha immunity.

Logic Block Diagram

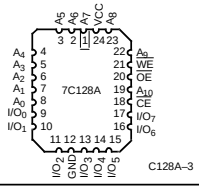


Pin Configurations

DIP/SOJ/SOIC Top View



LCC Top View



Selection Guide

		7C128A-15	7C128A-20	7C128A-25	7C128A-35	7C128A-45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	120	120	120	120	120
	Military	-	125	125	125	125
Maximum Standby Current (mA)	Commercial	40	20	20	20	20
	Military	-	20	20	20	20

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Document #: 38-05028 Rev. ** Revised August 24, 2001

Figure 1. First page of the memory data sheet.

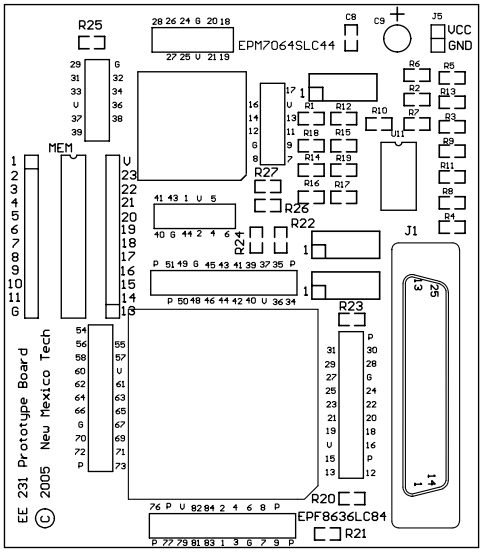

Figure 2. Diagram of the printed circuit card.

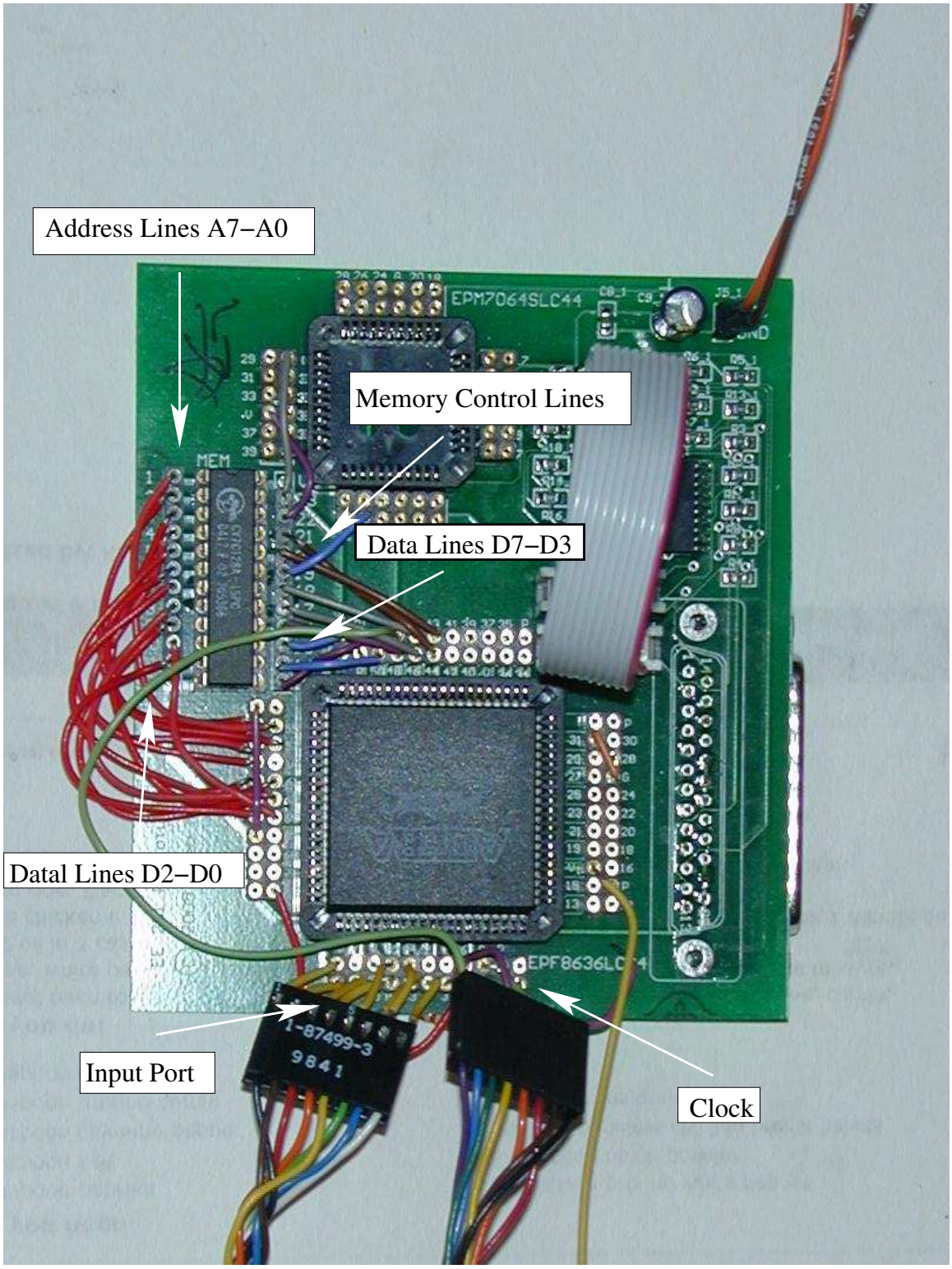

Figure 3. Picture of a wired computer.