

## EE 231L Lab 2

## Pre-Lab 3

1. Use Karnaugh maps to design a two-bit adder. This will be a four-input, three-output circuit which will add two two-bit numbers A and B, and produce a two-bit output Y and a one-bit carry C. How many gates are needed to achieve this design?
2. Look up the data sheet for the [74HC283](#) four-bit adder. How many gates were needed to implement this four-bit adder?
3. Write an Altera TDF program to implement the ALU. It will probably be best to use a CASE statement. Each individual function should be easy to write, if you tell AHDL to do the functions with 9 bits. For example, adding two eight-bit numbers to find an eight-bit sum and a one-bit carry can be coded as

$$(c,y[7..0]) = (0,a[7..0]) + (0,b[7..0]);$$

If the link to the 74HC283 above does not work, you can download the sheet at <http://www-s.ti.com/sc/ds/sn74hc283.pdf>.