EE 231L

Design with Altera Block Diagram/Schematic Files

Here is a brief tutorial for designing a digital circuit using an Altera Block Diagram/Schematic File. For a more detailed tutorial, look in the QUARTUS II help utility.

1. Find the QUARTUS II program. It should be a button in the lower-left corner of the screen next to the Start Menu. Open the QUARTUS II program.



2. From the **File** menu choose **New Project Wizard...** Enter the name of the working directory for the new project, or make a subdirectory for this lab if you haven't already done so. (Altera generates multiple files for each project. Having an organized file system will be VERY helpful when combining the separate elements for the final computer for EE 231 Lab). For your convenience, you can just type in the name of the project and ALTERA will use the same name for the top-level entity.

3. QUARTUS II will ask you for files to be included in this project. Leave this blank, and click Next.

4. Select which device you want to use for the implementation of your project. For this course we will use the EPF6016TC144-3 chip. First, go to the **Family** drop-down menu, and select **FLEX6000**. Click the button next to **Specific device selected in 'Available devices' list**. To narrow down the list of devices, go to the **Package** drop-down menu and select **TQFP**, then to the **Pin count** menu and select **144**, then to the **Speed grade** menu and select **3**. From the list of **Available devices**, select **EPF6016TC144-3**. Finally, click **Finish**..

5. From File menu choose New..., select the option Block Diagram/Schematic File, then OK. Now choose File | Save As and save with the same name as the project name, such as Boolean. The editor will attach a .BDF extension to the file.

6. Double click anywhere within the canvas. A dialog box will open showing a path to the directory where libraries are in QUARTUS II. Click on the + sign next to **libraries** to see the available libraries. The **primitives** library contains basic logic functions, such as AND, OR, and NOT gates. The **others/maxplus2** library contains more complex symbols, such as the common 7400 series logic. The **megafunctions** library has even more complex symbols, such as arithmetic operations, and symbols with variable numbers on inputs. (For example, if you need a 9-input AND gate, you can select **megafuntions/gates/lpm_and**, and will be able to specify the number of inputs to the AND gate.)

7. After placing the needed logic symbols on the canvas, enter symbols for the inputs and outputs (from the **primitives / pin** library). Double click on the **pin_name** label on each component in the circuit and enter the appropriate name. Make connections by clicking on a pin stub and dragging a wire to another pin stub. A design may look something like this:



8. Choose File | Save Project. After it saves with no errors, compile your design, and then simulate it using a waveform file:

Simulation Waveforms Simulation mode: Timing								
Master Time Bar: 18.775 ns Pointer: 25.93 ns Interval: 7.16 ns Start End:								
	Name	0 ps 18.775 ns	1.28 us	2.56 us	3.84 us	5.12 us	s 6.4 us	7.68 us
	x1 x2 x3 f							