# EE 308

## Exam 2

## April 1, 1999

Name: _____

You may use one page of notes and any of the Motorola data books. Show all work. Partial credit will be given. No credit will be given if an answer appears with no supporting work.

For all the problems in this exam, assume you are using an HC12 with a 16 MHz crystal, resulting in a 8 MHz processor clock.

Also assume that `hc12.h` has been included, so you can refer any register in the HC12 by name rather than by address.

1. The following questions concern writing C code.

   (a) Write some C code which will write the number 0x5a to the byte at address 0x0402.

   (b) Write some C code which will write the number 0x5aa5 to the two bytes at addresses 0x0400 and 0x0401.

   (c) Write some C code which will wait until the TOF bit of TFLG2 is set.

2. Below are the contents of the memory of an HC12:

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 09D0 | 10 | 23 | 3B | 7C | 10 | 04 | 86 | 80 | B7 | 10 | 25 | 3B | FC | 10 | 18 | F3 |
| 09E0 | 12 | 50 | FD | 10 | 18 | 86 | 40 | B7 | 10 | 23 | 3B | FC | 10 | 12 | DD | 02 |
| 09F0 | 86 | 02 | B7 | 10 | 23 | 3B | 7C | 10 | 03 | 86 | 40 | B7 | 10 | 25 | 3B | 86 |
| FFC0 | CC | 05 | 9F | CD | 99 | 03 | 84 | 9C | 01 | 9B | CC | 90 | 66 | FC | 93 | 30 |
| FFD0 | 7E | E3 | 4B | 7E | E5 | 38 | 21 | 54 | 05 | 83 | 09 | 34 | 2A | 38 | 3C | 03 |
| FFE0 | 41 | 38 | 66 | F2 | 7C | 13 | 37 | 0C | 25 | F2 | 0C | 38 | 5F | 1B | 42 | 1A |
| FFF0 | 7A | 26 | 21 | 13 | 6A | AA | 20 | 1F | 4B | 38 | 33 | 38 | 45 | 38 | 08 | 00 |

   (a) What is the address of the first instruction the HC12 will execute when coming out of reset?

   (b) What is the address of the first instruction of the timer overflow interrupt service routine?

   (c) What is the address of the first instruction of the pulse accumulator input edge interrupt service routine?

3. Below are the contents of the memory of an HC12:

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 09D0 | 10 | 23 | 3B | 7C | 10 | 04 | 86 | 80 | B7 | 10 | 25 | 3B | FC | 10 | 18 | F3 |
| 09E0 | 12 | 50 | FD | 10 | 18 | 86 | 40 | B7 | 10 | 23 | 3B | FC | 10 | 12 | DD | 02 |
| 09F0 | 86 | 02 | B7 | 10 | 23 | 3B | 7C | 10 | 03 | 86 | 40 | B7 | 10 | 25 | 3B | 86 |
| FFC0 | CC | 05 | 9F | CD | 99 | 03 | 84 | 9C | 01 | 9B | CC | 90 | 66 | FC | 93 | 30 |
| FFD0 | 7E | E3 | 4B | 7E | E5 | 38 | 21 | 54 | 05 | 83 | 09 | 34 | 2A | 38 | 3C | 03 |
| FFE0 | 41 | 38 | 66 | F2 | 7C | 13 | 37 | 0C | 25 | F2 | 0C | 38 | 5F | 1B | 42 | 1A |
| FFF0 | 7A | 26 | 21 | 13 | 6A | AA | 20 | 1F | 4B | 38 | 33 | 38 | 45 | 38 | 08 | 00 |

The HC12 registers have the following values:

| Reg | - | - |
|---|---|---|
| CCR | S X H I N Z V C<br>1 1 0 0 0 1 0 1 | |
| A:B | A3 | 92 |
| X | 82F2 | |
| Y | 12F7 | |
| SP | 09E7 | |
| PC | 0824 | |

Assume that the TOI interrupt has been enabled.

(a) List at least five things you need to do before enabling interrupts.

(b) Describe what happens to the HC12 between the time that the timer overflows and the HC12 starts executing the first instruction of the timer overflow interrupt service routine.

(c) Fill in any values in memory or registers which have changed in the HC12 gets to the first instruction in the timer overflow interrupt service routine. Leave blank any memory or register which has not changed value.

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 09D0 | | | | | | | | | | | | | | | | |
| 09E0 | | | | | | | | | | | | | | | | |
| 09F0 | | | | | | | | | | | | | | | | |

| Reg | - | - |
|---|---|---|
| CCR | S X H I N Z V C | |
| A:B | | |
| X | | |
| Y | | |
| SP | | |
| PC | | |

4. From the time the timer overflows to the time the HC12 starts executing the first instruction in the interrupt service routine, about how much time has elapsed.

5. Below are the values of some timer registers in the HC12:

| TIOS | TSCR | TCTL1 | TCTL2 | TCTL3 | TCTL4 | TMSK1 | TMSK2 | TFLG1 | TFLG2 |
|---|---|---|---|---|---|---|---|---|---|
| 32 | 80 | A4 | C2 | 5F | 76 | 2C | 84 | 52 | 00 |

(a) Which timer channels are being used for output compare?

(b) Which timer channel interrupts are enabled?

(c) What action is timer channel 2 set to perform? (I.e., if it is set up as input capture, which edge will it capture; if it is set up as output compare ; if it is set up as output compare what action will occur when `TCNT` equals `TC2`?)

(d) What action is timer channel 3 set to perform?

(e) What action is timer channel 4 set to perform?

(f) What action is timer channel 5 set to perform?

(g) Which timer flags are set?

(h) What is the timer prescaler set at – i.e., by what factor will the processor be divided before driving the `TCNT` register?

(i) How long (in seconds) will it take for the `TCNT` register to overflow?

6. The following questions pertain the the HC12 timer subsystem.

   (a) Timer channels 1 and 2 are both set up to capture the time of a falling edge. The timer prescaler is set to 3. When a falling edge occurs on channel 1, the number 0xD852 is latched into `TC1`. When a falling edge occurs on channel 2, the number 0x2712 is latched into `TC2`. How much time (in seconds) elapsed between the falling edge on channel 1 and the falling edge on chanel 2?

   (b) How do you clear a flag in the timer subsystem?

   (c) Write some C code to clear `C5F`, the flag for timer channel 5. Be sure your code does not clear any other timer flag which may be set.

   (d) What should you do to set the timer prescaler to a value of 3?

   (e) Write some C code to set the timer prescaler to a value of 3.

   (f) What should you do to set up timer channel 5 to function as an output compare, to toggle the output pin on a successful compare, and to generate an interrupt on a successful compare?

   (g) Write some C to set up timer channel 5 to function as an output compare, to toggle the output pin on a successful compare, and to generate an interrupt on a successful compare. Be sure your code does not change the function of any other timer channel.

   (h) The timer prescaler is set to 3. You are using timer channel 6 to generate a 2 kHz square wave. Timer channel 6 is set up to toggle the output on a successful compare. What number should you add to `TC6` after each successful comapre to get the 2 kHz square wave?

   (i) You are using the input capture function of the HC12 to measure a time difference of about 75 ms. What is the smallest value of the prescaler you can use to measure this time without `TCNT` wrapping around?

   (j) Write some C code to set the prescaler to the value of the above part?

7. The following items concern the pulse width modulation subsystem of the HC12.

   Use the values of the selected PWM registers below for Parts a-d.

| PWCLK | PWPOL | PWEN | PWSCAL0 | PWSCAL1 | PWPER0 | PWPER1 | PWDTY0 | PWDTY1 | PWCTL |
|---|---|---|---|---|---|---|---|---|---|
| 2D | 5F | 03 | 35 | 57 | C7 | 63 | 31 | 4F | 00 |

   (a) What is the period of the pulse width modulated signal generated on PWM channel 0?

   (b) What is the duty cycle of the pulse width modulated signal on PWM channel 0?

   (c) What is the period of the pulse width modulated signal generated on PWM channel 1?

   (d) What is the duty cycle of the pulse width modulated signal on PWM channel 1?

   (e) You want to set up PWM channel 3 to generate a pulse width modulated signal with a frequency of 600 Hz and a duty cycle of 40%. How will you set up the HC12 PWM registers to do this?

   (f) Write some C code to set up PWM channel 3 to generate a pulse width modulated signal with a frequency of 600 Hz and a duty cycle of 40%. Be sure your code does not change the function of any other PWM channel?

   (g) What is the advantage of using the PWM subsystem to generate a pulse width modulated signal rather than using timer channel 7 together with another of the timer output compare channels?