```c
#include <hc12.h>

main()
{
    DDRS = DDRS | 0xE0;           /* SS, SCLK, MOSI outputs */
    PORTS = PORTS | 0x80;         /* Deselect slave */

    SP0CR1 = 0x50;  /* 0 1 0 1 0 0 0 0
                       | | | | | | | |
                       | | | | | | | \____ MSB first
                       | | | | | | \______ multiple bytes with SS asserted
                       | | | | | \________ 0 phase (data valid on 1st edge)
                       | | | | \__________ 0 polarity (clock active low)
                       | | | \____________ Master mode
                       | | \______________ not open drain
                       | \________________ Enable SPI
                       \__________________ No interrupts
                    */

    SP0CR2 = 0;     /* Normal (not bi-directional) mode */

    SP0BR = 0x00;   /* 4 MHz SPI clock */

    PORTS = PORTS & ~0x80;         /* Select slave */

    SP0DR = 0x31;  /* 0 0 1 1 0 0 0 1
                            | |   | |
                            | |   | \____ Load DAC A
                            | |   \______ Don't load DAC B
                            | \__________ DAC A active
                            \____________ DAC B shut down
                    */
    while ((SP0SR & 0x80) == 0) ;  /* Wait for transmit complete */

    SP0DR = 51;                    /* Set DAC A for 1.0 V */
    while ((SP0SR & 0x80) == 0) ;  /* Wait for transmit complete */

    PORTS = PORTS | 0x80;          /* Deselect slave */

    PORTS = PORTS & ~0x80;         /* Select slave */

    SP0DR = 0x22;  /* 0 0 1 0 0 0 1 0               9
                            | |   | |
                            | |   | \____ Don't load DAC A
                            | |   \______ Load DAC B
                            | \__________ DAC A active
                            \____________ DAC B active
                    */
    while ((SP0SR & 0x80) == 0) ;  /* Wait for transmit complete */

    SP0DR = 189;                   /* Set DAC B for 3.7 V */
    while ((SP0SR & 0x80) == 0) ;  /* Wait for transmit complete */

    PORTS = PORTS | 0x80;          /* Deselect slave */
}
```