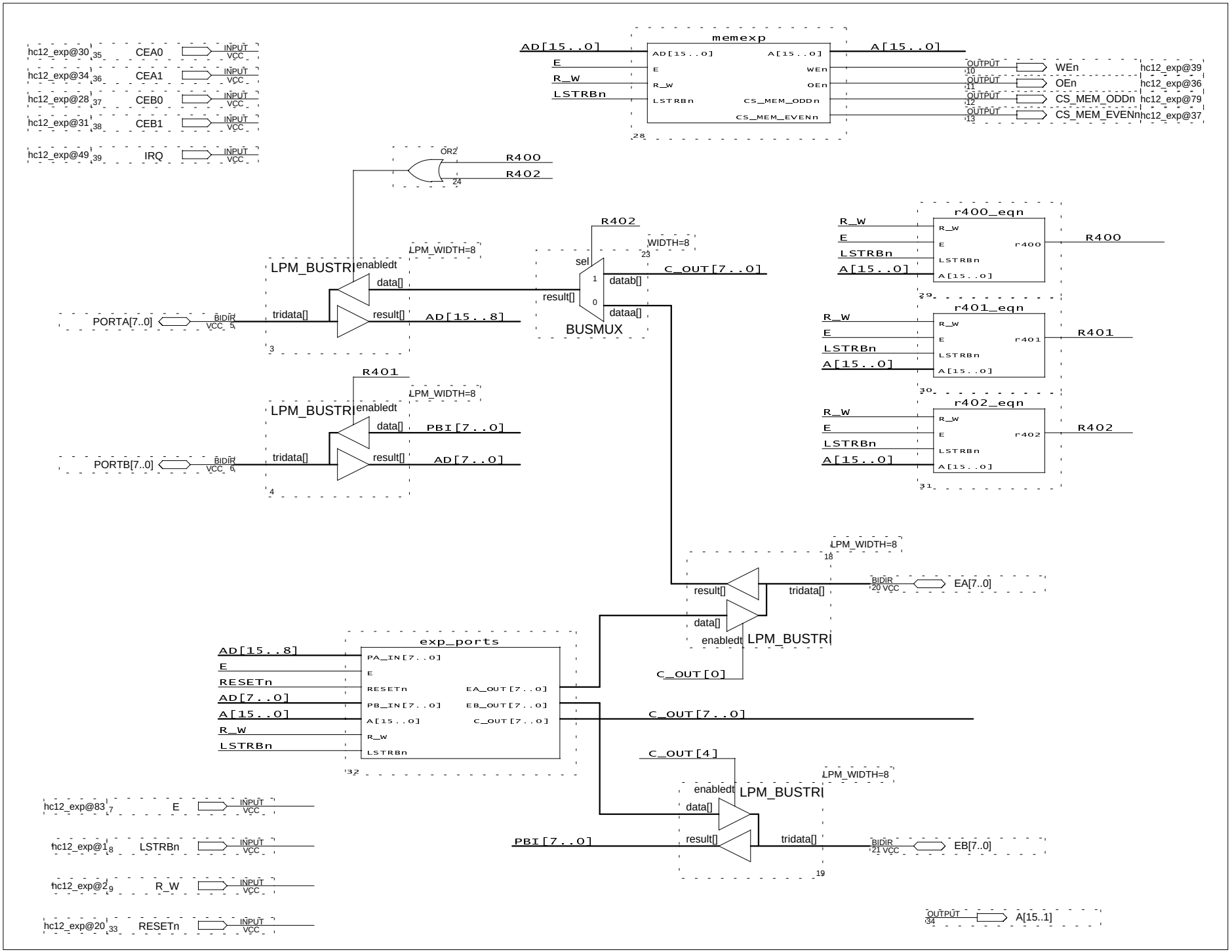
hc12_exp@30 35 CEA0 INPUT VCC
hc12_exp@34 36 CEA1 INPUT VCC
hc12_exp@28 37 CEB0 INPUT VCC
hc12_exp@31 38 CEB1 INPUT VCC
hc12_exp@49 39 IRQ INPUT VCC
memexp
AD[15..0]
E
R_W
LSTRBn
A[15..0]
WEn
OEn
CS_MEM_ODDn
CS_MEM_EVENn
OUTPUT 10 WEn hc12_exp@39
OUTPUT 11 OEn hc12_exp@36
OUTPUT 12 CS_MEM_ODDn hc12_exp@79
OUTPUT 13 CS_MEM_EVENn hc12_exp@37
28
OR2
R400
R402
24
LPM_WIDTH=8
LPM_BUSTR
enabledt
data[]
tridata[]
result[]
AD[15..8]
PORTA[7..0] BIDIR VCC 5
3
R402
WIDTH=8
23
sel
1
0
databa[]
dataa[]
C_OUT[7..0]
BUSMUX
r400_eqn
r400
r401_eqn
r401
r402_eqn
r402
29
30
31
R401
PBI[7..0]
AD[7..0]
PORTB[7..0] BIDIR VCC 6
4
18
EA[7..0] BIDIR 20 VCC
C_OUT[0]
exp_ports
PA_IN[7..0]
EA_OUT[7..0]
PB_IN[7..0]
EB_OUT[7..0]
C_OUT[7..0]
RESETn
32
C_OUT[4]
hc12_exp@83 7 E INPUT VCC
hc12_exp@1 8 LSTRBn INPUT VCC
hc12_exp@2 9 R_W INPUT VCC
hc12_exp@20 33 RESETn INPUT VCC
PBI[7..0]
EB[7..0] BIDIR 21 VCC
19
OUTPUT 34 A[15..1]