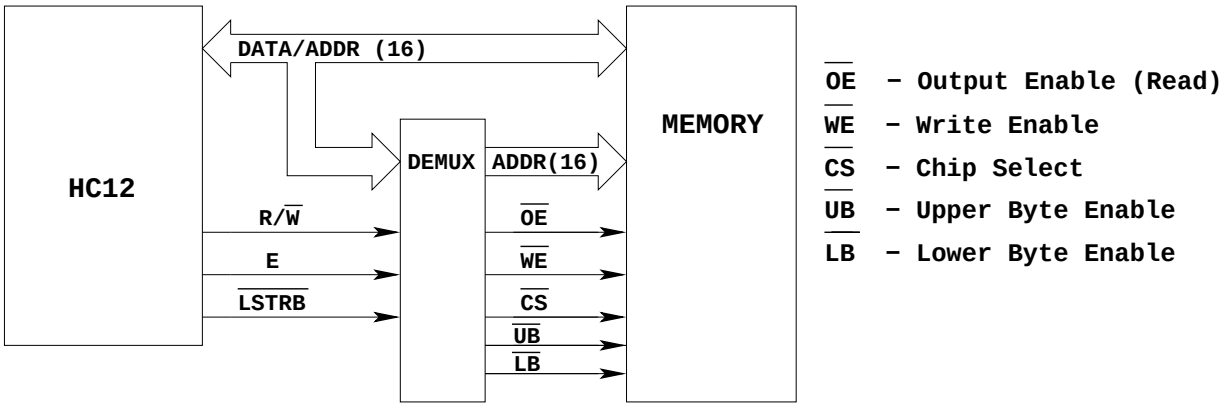
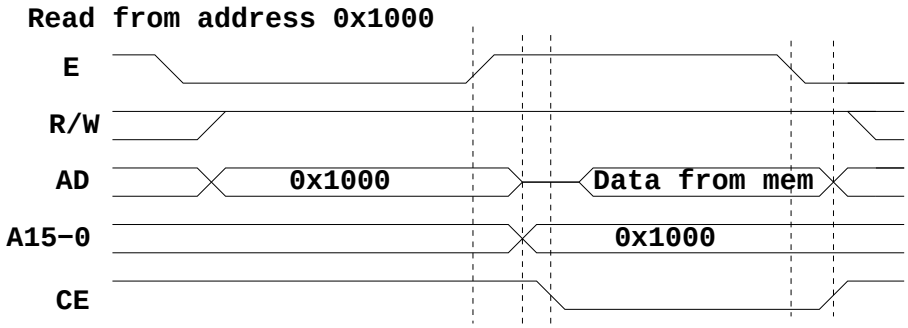
Timing Considerations for Interfacing to the External Bus

- There is an address latch, address decoder, and control decoder between the HC12 and the memory — this is often called ”glue logic”
- The glue logic in our memory expansion circuit is done in an Altera PLD
- The HC12 has timing specs which state when things will happen on its external bus
- The memory chip has timing specs which state when things will happen on its external bus
- It takes time for signals to propagate through the glue logic
- To make sure the memory and HC12 are compatible it is necessary to examine the timing specs for the HC12 and the memory chip, taking into account the time delays through the glue logic





From time E goes high it takes time before A15–0 comes out of Altera chip
One delay time, or about 12 ns
E high to new A15–0: about 12 ns

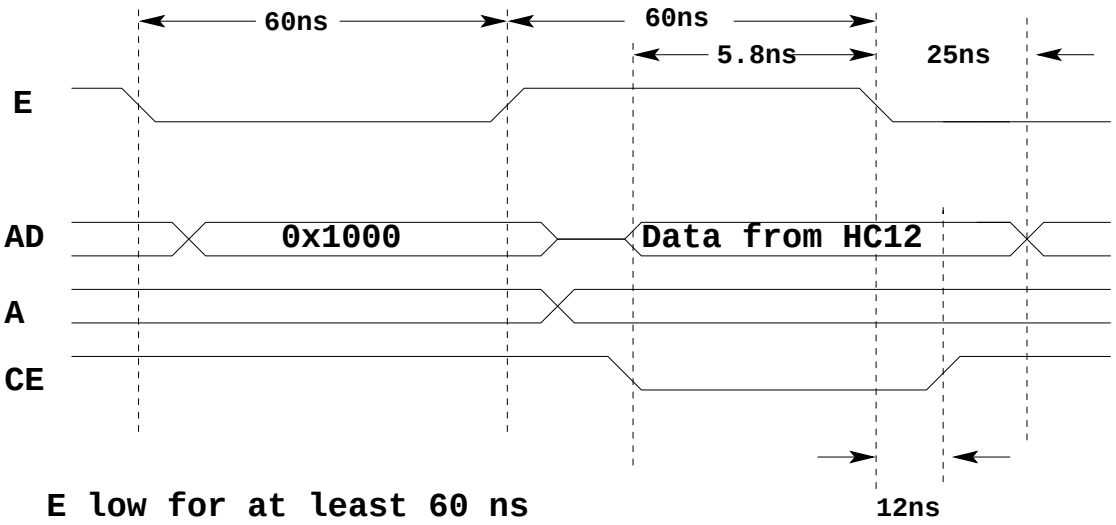
From time E goes high it takes time before CE goes low
One delay time, or about 12 ns, before A15–0 latched internally
One more delay time, or about 12 ns
E high to CE low: about 24 ns

From time E goes low it takes time before CE goes high
One delay time, or about 12 ns, before CE goes high
E low to CE high: about 12 ns

- When analyzing bus timing, the most critical thing to look for is data setup and data hold times
- When the HC12 does a write, the memory needs to latch the data on the low-to-high transition of CE, its Chip Enable
  - On write cycles the HC12 puts the data on the bus
  - Determine how long before CE goes high the data is on the bus — make sure this is longer than the Data Setup Time for the memory chip
  - Determine how long after CE goes high the data remains on the bus — make sure this is longer than the Data Hold Time for the memory chip
- When the HC12 does a read, the HC12 needs to latch the data on the high-to-low transition of E
  - On read cycles the memory puts the data on the bus
  - Determine how long before E goes low the data is on the bus — make sure this is longer than the Data Setup Time for the HC12
  - Determine how long after E goes low the data remains on the bus — make sure this is longer than the Data Hold Time for the HC12
- One other item to look for is the Address Access Time — how long it takes from the time the memory chip sees a new address until it can access data internally
- From the time a new address is available until E goes low is about 60 ns
  - To run at full speed the HC12 needs to use memory chips with access times less than 60 ns
  - The chip we are using has a 12 ns access time
- If you have to use a slower memory chip it is possible to slow down the HC12
  - You can use a slower crystal, which slows everything down
  - You can add clock stretches, which slows down accesses to devices connected to the external address/data bus

HC12 and Glue Logic Timing – Write

- Consider the signals on the bus when the HC12 writes to the memory chip



E low for at least 60 ns
E high for at least 60 ns
HC12 puts data on bus at least 5.8 ns before E goes low
HC12 keeps data on bus at least 25 ns after E goes low
CE goes high 12 ns after E goes low

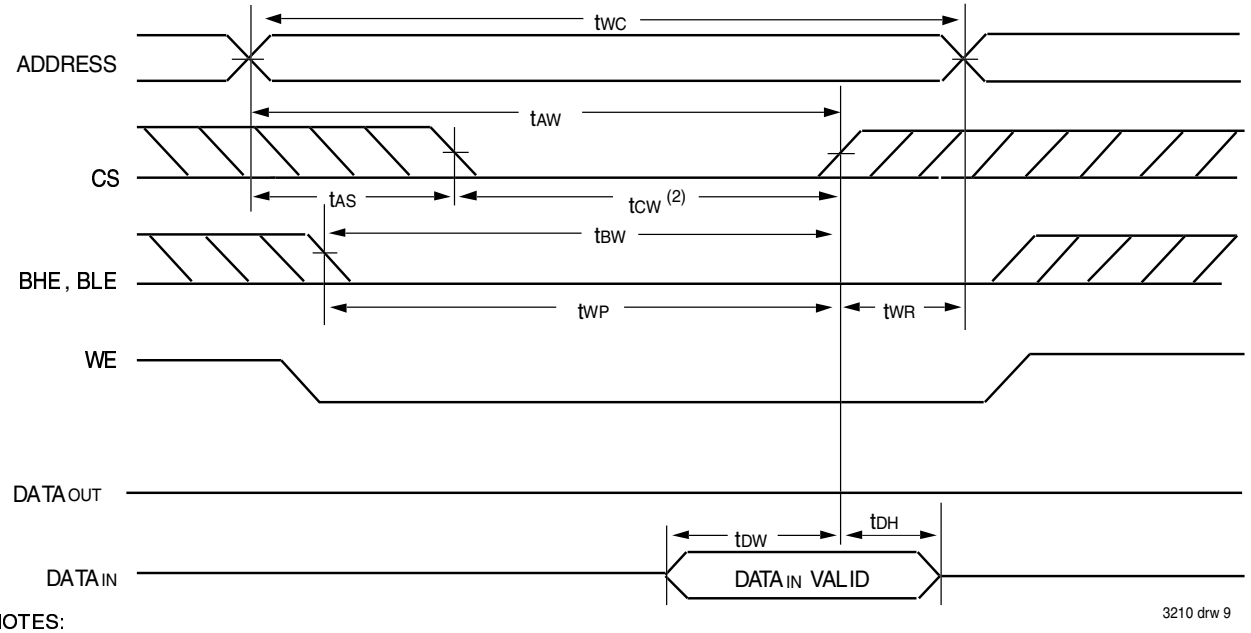
Memory must need setup time of less than 5.8 + 12 = 17.8
Memory must need hold time of less than 25 − 12 = 13 ns

- The new address is available about 60 ns before CE goes high
  - We need a memory chip with a write address access time of less than 60 ns
- The data is on the bus about 18 ns before CE goes high
  - We need a memory chip with a write setup time of less than 18 ns
- The data is kept on the bus for about 13 ns after CE goes high
  - We need a memory chip with a write hold time of less than 13 ns

AC Electrical Characteristics (Vcc = 5.0V + 10 %, Commercial and Industrial Range)

Symbol	Parameter	71016S12		71016S15		71016S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End of Write	9	—	10	—	12	—	ns
t_{CW}	Chip Select Low to End of Write	9	—	10	—	12	—	ns
t_{BW}	Byte Enable Low to End of Write	9	—	10	—	12	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WR}	Address Hold from End of Write	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	9	—	10	—	12	—	ns
t_{DW}	Data Valid to End of Write	7	—	8	—	10	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{OW}[1]	Write Enable High to Output in Low-Z	1	—	1	—	1	—	ns
t_{WHZ}[1]	Write Enable Low to Output in High-Z	—	6	—	6	—	8	ns

Timing Waveform of Write Cycle No. 2 (1)



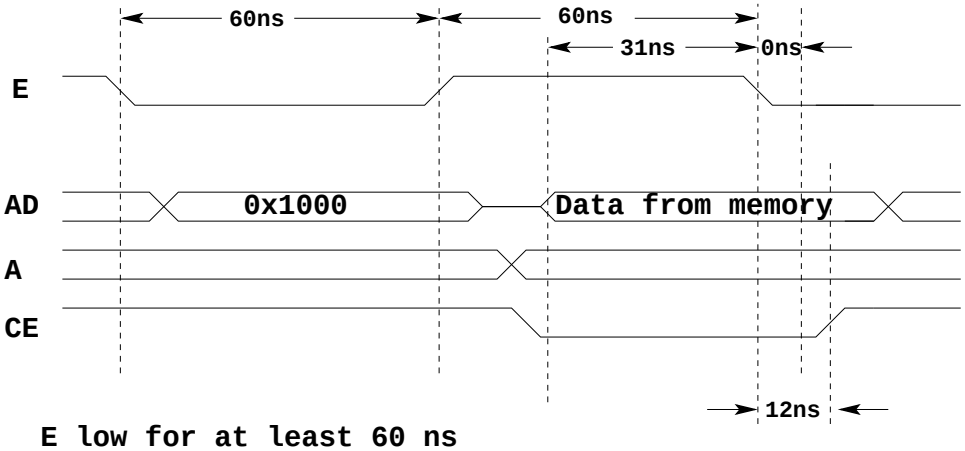
NOTES:
1. A write occurs during the overlap of a LOW CS, LOW BHE or BLE, and a LOW WE.
2. OE is continuously HIGH. If during a WE controlled write cycle OE is LOW, then t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If OE is HIGH during a WE controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP}.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CS LOW or BHE and BLE LOW transition occurs simultaneously with or after the WE LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured ±200mV from steady state.

Write Timing of the IDT71016 Memory Chip

- For the 12 ns IDT7016 the write address access time is 9 ns, less than the 60 ns provided by the HC12 and glue logic
- For the 12 ns IDT7016 the write setup time is 7 ns, less than the 18 ns provided by the HC12 and glue logic
- For the 12 ns IDT7016 the write setup hold is 0 ns, less than the 13 ns provided by the HC12 and glue logic
- **The IDT71016 write cycle is compatible with the HC12 timing**

- Consider the signals on the bus when the HC12 reads from the memory chip

HC12 READ TIMING − EXPANDED MODE



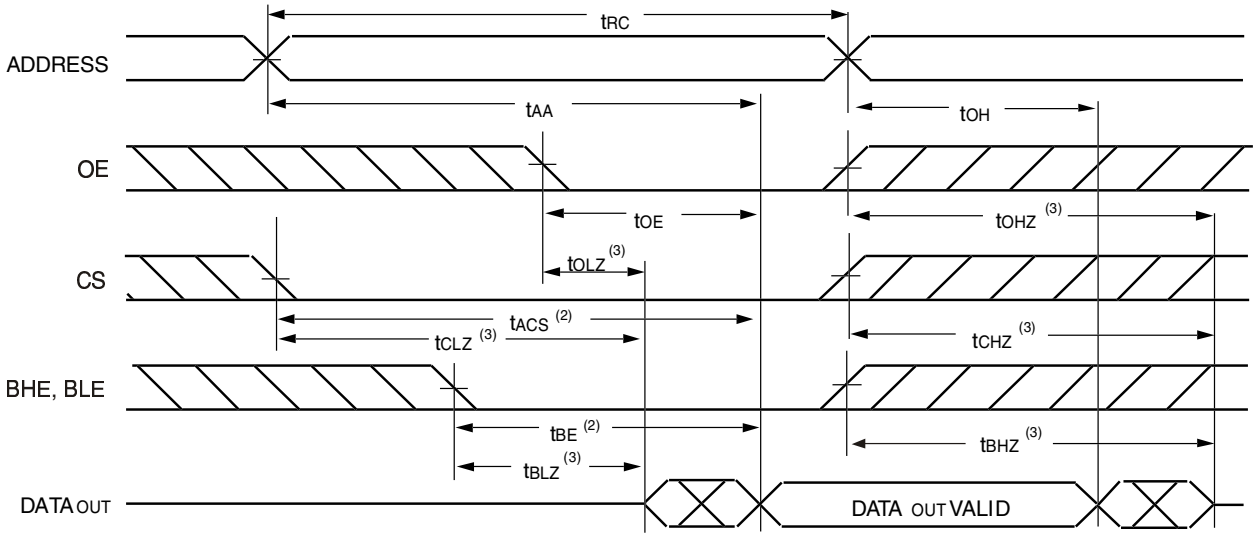
E low for at least 60 ns
E high for at least 60 ns
Memory must have data on bus 31 ns before E goes low
Memory must keep data on bus 0 ns after E goes low

- The new address is available about 60 ns before CE goes high
  - We need a memory chip with a read address access time of less than 60 ns
- The data needs to be on the bus 31 ns before E goes low
  - After E goes high, CE goes low 24 ns later
  - The memory needs to put the data on the bus 29 ns after E goes high
  - The memory chip will have the data on the bus 24 ns + time from CE low to memory on bus
  - Need memory chip with CE to output enable time of less the 5 ns
- The data needs to be kept on the bus for at least 0 ns after E goes low
  - From the time E goes low to CE high is about 12 ns
  - We need a memory chip which not remove data 12 ns before CE goes high (-12 ns)
  - Every memory chip will keep data on the bus until after CE goes high, so there is no problem here

AC Electrical Characteristics (Vcc = 5.0V ± 10 %, Commercial and Industrial Range)

Symbol	Parameter	71016S12		71016S15		71016S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	12	—	15	—	20	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	20	ns
t_{ACS}	Chip Select Access Time	—	12	—	15	—	20	ns
t_{CLZ}	Chip Select Low to Output in Low-Z	4	—	5	—	5	—	ns
t_{CHZ}	Chip Select High to Output in High-Z	—	6	—	6	—	8	ns
t_{OE}	Output Enable Low to Output Valid	—	7	—	8	—	10	ns
t_{OLZ}	Output Enable Low to Output in Low-Z	0	—	0	—	0	—	ns
t_{OHZ}	Output Enable High to Output in High-Z	—	6	—	6	—	8	ns
t_{OH}	Output Hold from Address Change	4	—	4	—	5	—	ns
t_{BE}	Byte Enable Low to Output Valid	—	7	—	8	—	10	ns
t_{BLZ}	Byte Enable Low to Output in Low-Z	0	—	0	—	0	—	ns
t_{BHZ}	Byte Enable High to Output in High-Z	—	6	—	6	—	8	ns

Timing Waveform of Read Cycle No. 2 (1)

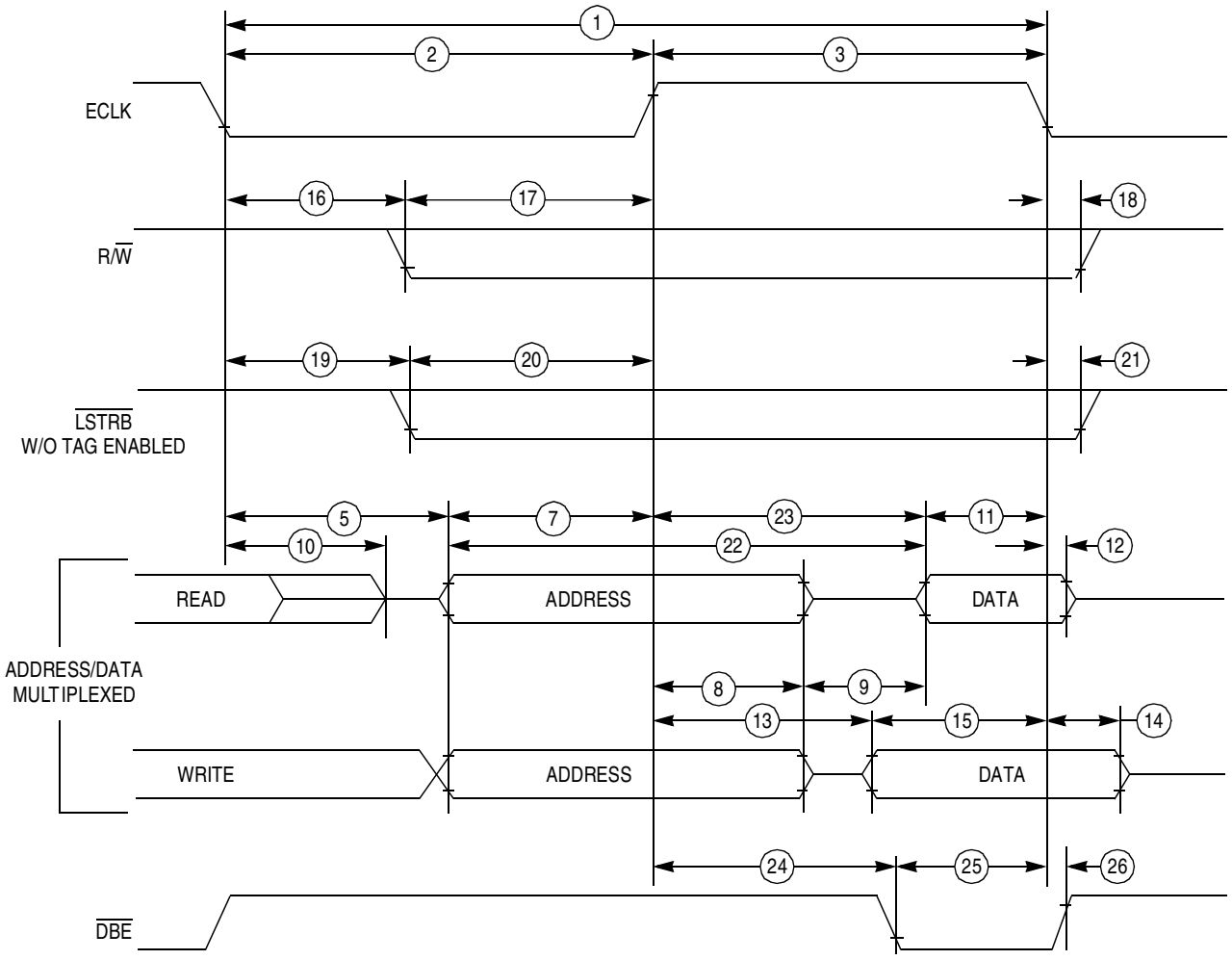


3210 drw 07

NOTES:
1. WE is HIGH for Read Cycle.
2. Address must be valid prior to or coincident with the later of CS, BHE, or BLE transition LOW; otherwise t_{AA} sets the limiting parameter.
3. Transition is measured ±200mV from steady state.

Read Timing of the IDT71016 Memory Chip

- For the 12 ns IDT7016 the read address access time is 12 ns, less than the 60 ns required
- For the 12 ns IDT7016 the read CE to output enable time is 12 ns, slightly longer the the 5 ns required by the HC12 and glue logic — Does Not Quite Meet Specs the 5 ns required
- For the 12 ns IDT7016 the read hold time is 6 ns, more than the -12 ns required — Meets Specs
- **The IDT71016 read cycle is almost (but not completely) compatible with the HC12 timing**
- The timing specs given in data sheets are worst-case specs — the manufacturer guarantees all parts will meet these specs under all conditions the chip is speced for
- Timing within a few ns will almost certainly work in most cases
- You should **not** use the given setup (HC12, 12 ns Altera, 12 ns IDT71016) in critical applications — it may not work under some circumstances
- To ensure it will work you could either
  - Go to a faster memory chip (with a 5 ns CE to output enable time)
  - Go to a faster Altera chip (an Altera with 7 ns delay would work)
  - Add a clock stretch — this will increase the length of time E is high by one clock cycle, or 125 ns, which will increase the time the data is on the bus by 125 ns, to a total of 130 ns, far longer than the 7 ns the HC12 needs
  - Reduce the clock speed — this will slow down all operations with the HC12



Note: Measurement points shown are 20% and 70% of V_{DD}.

Figure 19-10. Multiplexed Expansion Bus Timing Diagram

19.16 Multiplexed Expansion Bus Timing

NOTE: *Use of the multiplexed expansion bus at 8 MHz is discouraged due to TAD delay factors.*

Num	Characteristic[1], [2], [3], [4], [5]	Delay	Symbol	8 MHz		2 MHz		Unit
				Min	Max	Min	Max	
—	Frequency of operation (E-clock frequency)	—	f_o	dc	8.0	dc	8.0	MHz
1	Cycle time $t_{cyc} = 1/f_o$	—	t_{cyc}	125	—	500	—	ns
2	Pulse width, E low $PW_{EL} = t_{cyc}/2 + \text{delay}$	–4	PW_{EL}	59	—	246	—	ns
3	Pulse width, E high[6] $PW_{EH} = t_{cyc}/2 + \text{delay}$	–2	PW_{EH}	59	—	248	—	ns
5	Address delay time $t_{AD} = t_{cyc}/4 + \text{delay}$	27	t_{AD}	—	67.5	—	152	ns
7	Address valid time to ECLK rise $t_{AV} = PW_{EL} - t_{AD}$	—	t_{AV}	–6.2	—	94	—	ns
8	Multiplexed address hold time $t_{MAH} = t_{cyc}/4 + \text{delay}$	–18	t_{MAH}	13	—	107	—	ns
9	Address hold to data valid	—	t_{AHDS}	30	—	20	—	ns
10	Data hold to high impedance $t_{DHZ} = t_{AD} - 20$	—	t_{DHZ}	—	45.2	—	132	ns
11	Read data setup time	—	t_{DSR}	31.2	—	25	—	ns
12	Read data hold time	—	t_{DHR}	0	—	0	—	ns
13	Write data delay time	—	t_{DDW}	—	62.5	—	165	ns
14	Write data hold time	—	t_{DHW}	25	—	20	—	ns
15	Write data setup time[6] $t_{DSW} = PW_{EH} - t_{DDW}$	—	t_{DSW}	5.8	—	83	—	ns
16	Read/write delay time $t_{RWD} = t_{cyc}/4 + \text{delay}$	18	t_{RWD}	—	57.5	—	143	ns
17	Read/write valid time to E rise $t_{RWV} = PW_{EL} - t_{RWD}$	—	t_{RWV}	3.8	—	103	—	ns
18	Read/write hold time	—	t_{RWH}	25	—	20	—	ns
19	Low strobe[7] delay time $t_{LSD} = t_{cyc}/4 + \text{delay}$	18	t_{LSD}	—	57.5	—	143	ns
20	Low strobe[7] valid time to E rise $t_{LSV} = PW_{EL} - t_{LSD}$	—	t_{LSV}	3.8	—	103	—	ns
21	Low strobe[7] hold time	—	t_{LSH}	25	—	20	—	ns
22	Address access time[6] $t_{ACCA} = t_{cyc} - t_{AD} - t_{DSR}$	—	t_{ACCA}	—	27.6	—	323	ns
23	Access time from E rise[6] $t_{ACCE} = PW_{EH} - t_{DSR}$	—	t_{ACCE}	—	27.8	—	223	ns
24	$\overline{DBE}$ delay from ECLK rise[6] $t_{DBED} = t_{cyc}/4 + \text{delay}$	8	t_{DBED}	—	57.5	—	133	ns
25	$\overline{DBE}$ valid time $t_{DBE} = PW_{EH} - t_{DBED}$	—	t_{DBE}	11.8	—	115	—	ns
26	$\overline{DBE}$ hold time from ECLK fall	—	t_{DBEH}	–3	10	–3	10	ns

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted
2. All timings are calculated for normal port drives.
3. Crystal input is required to be within 45% to 55% duty.
4. Reduced drive must be off to meet these timings.
5. Unequalled loading of pins will affect relative timing numbers.
6. This characteristic is affected by clock stretch.
   Add $N \times t_{cyc}$ where N = 0, 1, 2, or 3, depending on the number of clock stretches.
7. Without TAG enabled

Clock Stretches on the HC12

- You can add one, two, or three clock stretches to the HC12
- Each clock stretch adds one clock cycle to the length of time E is high
- It does not change the amount of time E is low
  - With one clock stretch, E is low for at least 60 ns, and high for at least 60 + 125 = 185 ns
  - With two clock stretches, E is low for at least 60 ns, and high for at least 60 + 250 = 310 ns
  - With three clock stretches, E is low for at least 60 ns, and high for at least 60 + 375 = 430 ns
- With clock stretches can use slower memory chips (such as 250 ns ROMS) with the HC12

The HC12B32 in Expanded Mode at 8 MHz

- At 8 MHz the HC12 has an Address Valid to ECLK rise time of -6.2 ns
- This means that, under some circumstances, the address may not be on the bus until 6.2 ns **after** ECLK goes high
- This means that, under these circumstances, an address latch cannot work
- This cannot be fixed by adding E-clock stretches, since ECLK stretches do not change the amount of time E is low
- Because of this the Motorola data sheet states:
  "Use of the multiplexed expansion bus at 8 MHz is discouraged due to TAD delay factors"
- Under most circumstances memory expansion will work with an 8 MHz bus
- For commercial applications you should not use the HC12B32 in expanded mode running at 8 MHz
  - Use a slower clock — a 4 MHz bus speed will work fine
  - Use an HC12 which does not multiplex the address and data buses, such as the HC12A4