EE 308 – Homework 8
Due March 21, 2005

For all problems below assume your are using a MCS12DP256 chip with a 24 MHz bus clock and a 4 MHz oscillator clock.

1. The table below shows some values in the HCS12’s PWM registers:

<table>
<thead>
<tr>
<th>PWMCAE</th>
<th>PWMCLK</th>
<th>PWMPRCLK</th>
<th>PWMPOL</th>
<th>PWME</th>
<th>PWMSCLA</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>0x02</td>
<td>0x84</td>
<td>0xFF</td>
<td>0x0F</td>
<td>0x2A</td>
</tr>
<tr>
<td>PWMSCLB</td>
<td>PWMPER0</td>
<td>PWMPER1</td>
<td>PWMDTY0</td>
<td>PWMDTY1</td>
<td>PWMCTL</td>
</tr>
<tr>
<td>0xA5</td>
<td>0x64</td>
<td>0xC8</td>
<td>0x32</td>
<td>0x51</td>
<td>0x00</td>
</tr>
</tbody>
</table>

(a) What is the period (in seconds) of the pulse width modulated signal generated on PWM channel 0?
(b) What is the duty cycle (in percent) of the pulse width modulated signal on PWM channel 0?
(c) What is the period (in seconds) of the pulse width modulated signal generated on PWM channel 1?
(d) What is the duty cycle (in percent) of the pulse width modulated signal on PWM channel 1?

2. You want to set up PWM channel 2 to generate a pulse width modulated signal with a frequency of 5 kHz and a duty cycle of 60%. How will you set up the HCS12 PWM registers to do this? Indicate which clock mode you will use, and the values of PCKB (and PWMSCLB, if you use clock mode 1).

3. Write some C code to set up PWM channel 2 to generate a pulse width modulated signal with a frequency of 5 kHz and a duty cycle of 60%. Be sure your code does not change the function of any other PWM channel?

4. Write a C program which does the following:

   (a) Set up one of the PWM channels for a frequency of 5 kHz.
   (b) Enable timer subsystem for an overflow rate of at least 25 ms.
   (c) Set up one of the timer channels for Input Capture, with interrupts enabled.
   (d) Write an Input Capture interrupt service routine which latches the time of the rising edge on the timer channel you are using.
   (e) Write an infinite loop which does the following:

       i. Read the state of four DIP switches connected to Port B. Set the PWM duty cycle based on those switches as follows:
Have a table of integer values which gives the duty cycles closest to those listed in
the table.

ii. Print out the time difference between the last two input capture edges to the screen.