EE 308

Final Exam

May 7, 2001

Name: _____

You may use any of the Motorola data books, notes from the EE 308 web page, and your lab notebook. Show all work. Partial credit will be given. No credit will be given if an answer appears with no supporting work.

No calculators are allowed for this part of the exam.

1. Fill in all missing entries in the following table. Use an 8-bit word size.

Hex	Binary	Unsigned Decimal	Signed Decimal
9F			
		23	
			-23
			127

2. Do the following operations on eight-bit numbers. Indicate the eight-bit answer, and the state of the C, V, N and Z flags after the operation.

	6C + 7A	6C + 94	CD + EF	1C - 85	85 - 1C
Answer					
C					
V					
N					
Z					

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For all the questions below, assume the 68HC12 has a 16 MHz crystal which results in an 8 MHz processor clock.

For all C code you write assume hc12.h has been included so you can refer to all registers by name.

1. Consider the following program fragment:

Address			Op Code & Operands	Addressing Mode	Cycles
----	CODE: section .text		----	----	----
----	org	$1000	----	----	----
1000	lds	#$8000	CF 80 00	IMM	2
	ldaa	$8000			
	anda	2,-X			
	incb				
	staa	$75			
	jsr	$1085			

(a) Fill in the above table. In the column labeled `Address`, fill in the address of the first byte of the instruction. In the columns labeled `Op Codes & Operands` show the op codes and operands (as hex numbers). In the column labeled `Addressing Mode` indicate the addressing mode used by the instruction. In the column labeled `Cycles` indicate the number of cycles needed to execute the instruction.

(b) How many bytes of memory does the code fragment occupy? Include all 7 instructions.

(c) How many microseconds will it take the fragment to execute on an HC12 with a 8 MHz processor clock? Include all 7 instructions.

(d) For the same instructions show the values of each of the registers and flags after execution of the instruction. You do not have to put down a value if the value did not change.

Inst	A	B	X	Y	SP	PC	N	Z	V	C
	FF	FF	7FF0	8008	FFFF	1000	1	1	1	1
lds #$8000										
ldaa $8000										
anda 2,-X										
incb										
staa $75										
jsr $1085										

The table below shows some values in memory which will be needed to do the above.

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
7FE0	10	23	3B	7C	10	04	86	80	B7	10	25	3B	FC	10	18	F3
7FF0	12	50	FD	10	18	86	40	B7	10	23	3B	FC	10	12	DD	02
8000	86	02	B7	10	23	3B	7C	10	03	86	40	B7	10	25	3B	86

2. The following tables show the values of an HC12's registers and some of its memory.

Reg	–	–
CCR	S X H I N Z V C	
	1 0 0 0 1 0 0 1	
A:B	A3	92
X	82F2	
Y	12F7	
SP	208D	
PC	31F4	

TIOS	OC7M	OC7D	TSCR	TCTL1	TCTL2	TCTL3	TCTL4	TMSK1	TMSK2	TFLG1	TFLG2
96	47	5F	80	5F	93	7A	A4	5C	82	08	80

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0800	C6	05	CE	09	00	DD	5A	33	6A	05	08	53	26	F7	3F	CE
0810	E0	00	CD	00	00	E6	00	0F	00	01	02	19	ED	08	8E	E0
0820	20	25	F2	7A	09	00	3F	CF	0A	00	15	FA	00	01	5F	A0
0830	01	3F	C6	80	5B	86	C6	03	5B	8D	C6	FF	5B	02	4C	80
FFD0	AB	20	CD	30	EF	40	F5	50	56	60	78	70	98	80	20	90
FFE0	84	A0	3F	B0	F3	D0	74	F0	9A	12	C2	10	A7	20	D9	30
FFF0	A5	3C	10	59	3A	43	08	19	93	7A	A4	5C	82	08	89	A0

(a) What is the address of the first instruction the HC12 will execute after a reset? _____

(b) What is the address of the Timer Channel 2 interrupt service routine? _____

(c) What interrupts are enabled in the timer subsystem? _____

(d) How long (in seconds) will it take for the TCNT register to overflow? _____

(e) What function is Timer Channel 2 set up for (input capture or output compare? _____

(f) What function will Timer Channel 2 perform (if IC, will it capture rising, falling, both, or none;

   if OC, will it set, clear, toggle, or is it disconnected)? _____

(g) What function is Timer Channel 3 set up for (input capture or output compare? _____

(h) What function will Timer Channel 3 perform (if IC, will it capture rising, falling, both, or none;

   if OC, will it set, clear, toggle, or is it disconnected)? _____

(i) When using an input capture function, the first edge is captured when `TCNT = 0xC123`, and the second edge is captured when `TCNT = 0x4CBA`. It is known that the total number of timer ticks is less than `0xFFFF`.

     i. How many timer ticks were there between the two edges? _____

     ii. How much time (in seconds) was there between the two edges? Use the values in the timer

     registers on the previous page, if needed. _____

(j) Write some C code to do the following: Set up timer channel 4 to function as an output compare, set pin Port T4 on a successful compare, and generate an interrupt on a successful compare. Be sure you do not change the function of any other timer channel when you set up timer channel 4.

(k) Write some C code to clear the timer channel 4 flag. Make sure you do not clear any other flag while doing so.

(l) Show what will be in the HC12 registers when it starts executing the first instruction of the timer channel 4 interrupt service routine, and show what has happened to the stack. (Use the table from the previous page as the initial values of the registers.) For the stack contents, indicate the addresses of the stack which will be changed, and the values which will be in those addresses.

Reg	–	–	Stack Contents
	S X H I N Z V C		
CCR			
A:B			
X			
Y			
SP			
PC			

(m) What assembly language instruction should you use when you exit an interrupt service routine? Why?

3. An HC12 is connected to to a 16-bit A/D converter as shown below. The A/D converter sends 16 bits of data to the HC12. The SPI timing used by the A/D converter is also shown.
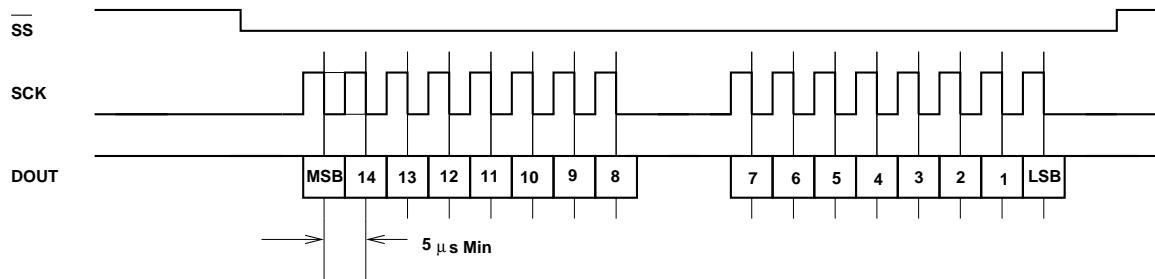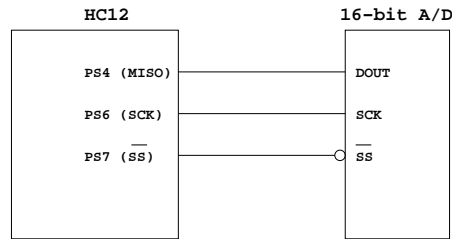
(a) Write some C code to set up the HC12 to communicate with the A/D converter, without using interrupts. Make sure to comment your code to explain what you did.

(b) Assume that the SPI has been properly set up to communicate with the A/D converter. Write some C code to read a conversion and assign it to a 16-bit variable called `data`.

(c) How do you clear the SPI flag?

4. Here are some questions about other subsystems of the HC12.

   (a) How should you set up the A/D control registers to have the HC12 do the following: Operate in 10-bit mode, perform eight conversions of the signal on port PAD5, then stop. Write some C code to do this.

   (b) An HC12 has $V_{RL} = 0V$ and $V_{RH} = 4V$. The input on Pin 5 of Port E is 2.75 V. What will be in the A/D result register ADR5 after the conversion initiated above?

   (c) You want to use Channel 3 of the HC12 PWM subsystem to generate a 100 Hz PWM signal with a 25% duty cycle. What would you write to the PWM registers to do this? Be sure to comment your code to indicate what you did.

5. The following question concerns the HC12 in expanded mode.

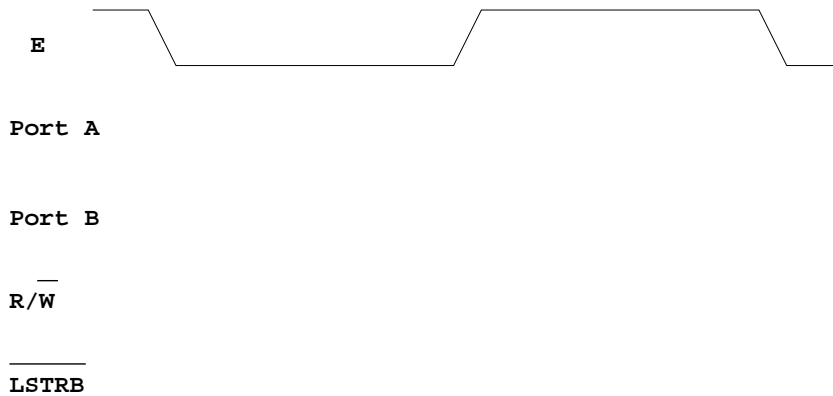   The following table shows some values in the HC12 memory:

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2080	01	3F	C6	80	5B	86	C6	03	5B	8D	C6	FF	5B	02	4C	80

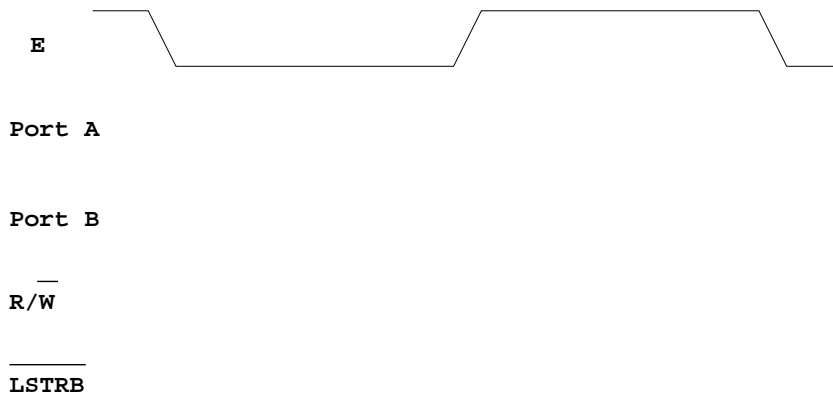   Show what will be on the address/data bus and the control lines when the HC12 does the following:

   (a) Writes a 0xAA to address 0x2080.

   E

   Port A

   Port B

   R/W

   LSTRB
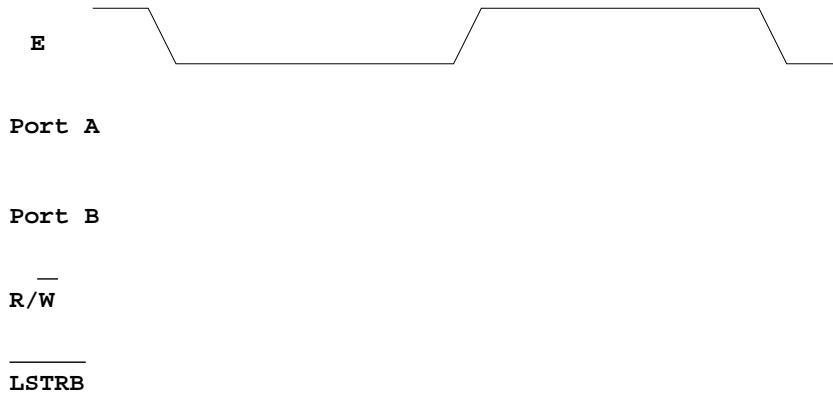
   (b) Writes a 0x55AA to the two bytes at addresses 0x2082 and 0x2083.

   E

   Port A

   Port B

   R/W

   LSTRB

   (c) Reads a single byte from addresses 0x2089.

   E

   Port A

   Port B

   R/W

   LSTRB

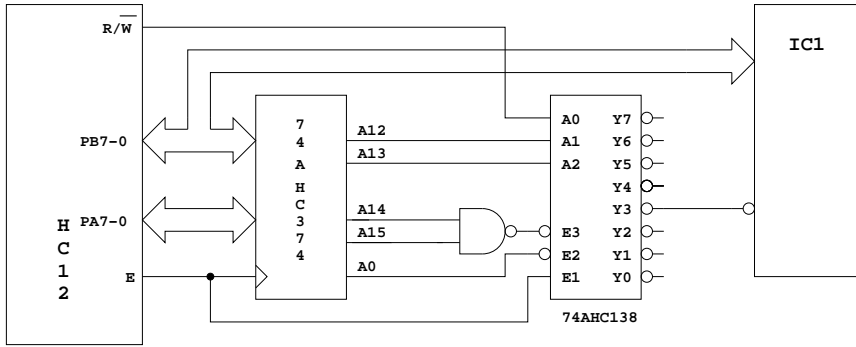6. Of the three figures below, only one will work reliable in expanded mode.
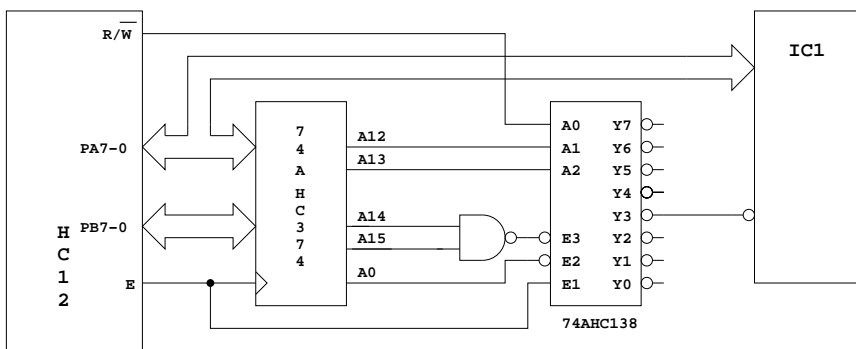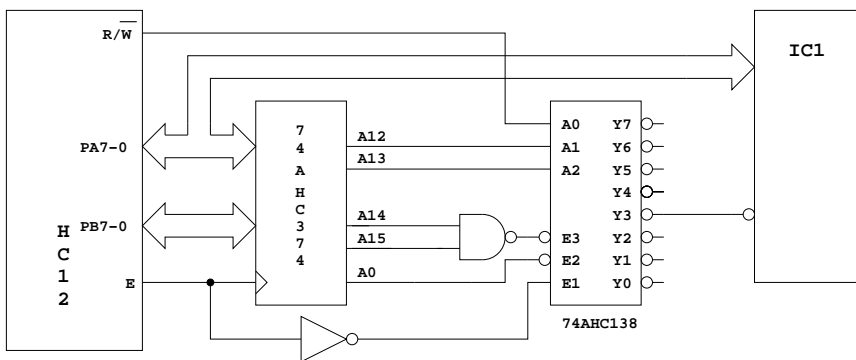

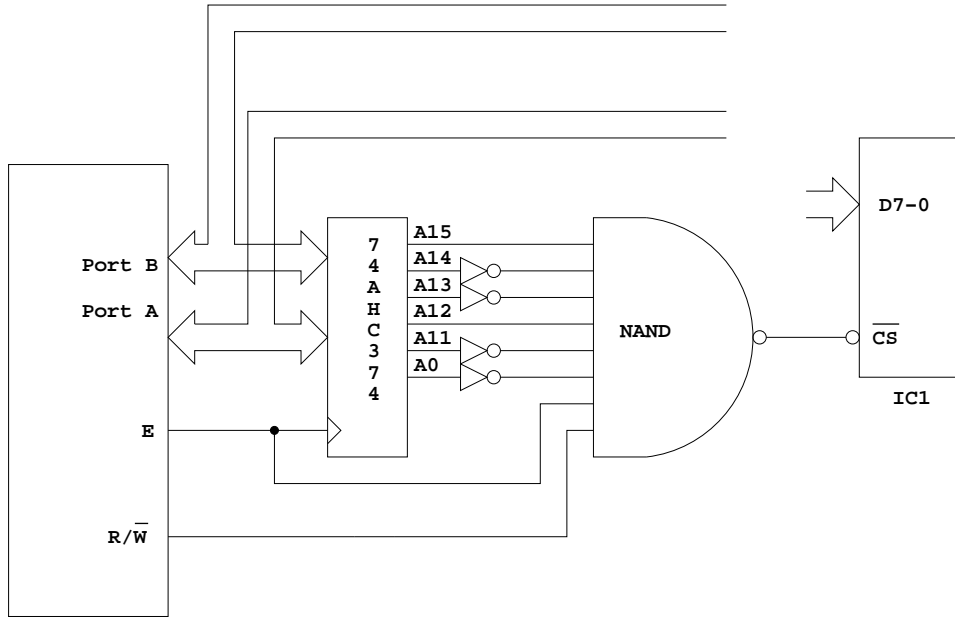**Figure (a)**

Figure (b)

Figure (c)

(a) Figure (a): Will this work? If not, why not?

(b) Figure (b): Will this work? If not, why not?

(c) Figure (c): Will this work? If not, why not?

7. The following shows the HC12 interfaced to a peripheral chip:

(a) Is the peripheral in input or output chip?Why?

(b) What range of addresses will select the peripheral?

(c) Should you connect the data lines for the peripheral to Port A or Port B? Why?

(d) Assume that the peripheral is an input. Answer the following timing questions, assuming that the delay through each of the glue chips is 10 ns.

    i. How long will it be from the time E goes high until $\overline{CS}$ goes low, if there is no E-clock stretch?

    _____

    ii. How long will it be from the time E goes high until $\overline{CS}$ goes low, if there are two E-clock stretches? _____

    iii. How long will it be from the time the E goes high until the chip puts its data on the bus, if there is no E-clock stretch? _____

    iv. How long will it be from the time the E goes high until the chip puts its data on the bus, if there there are two E-clock stretches? _____

    v. How long will it be from the time E goes low until the chip removes data from the bus, if there is no E-clock stretch? _____

    vi. How long will it be from the time E goes low until the chip removes data from the bus, if there are two E-clock stretches? _____

    vii. If the data access time for the peripheral chip is 30 ns (max), will the HC12 setup time be met with no E-clock stretch? _____

    viii. If the data access time for the peripheral chip is 30 ns (max), will the HC12 setup time be met with two E-clock stretches? _____

    ix. If the data hold time for the peripheral chip is 15 ns (min), will the HC12 setup time be met with no E-clock stretch? _____

    x. If the data setup time for the peripheral chip is 15 ns (min), will the setup time be met with two E-clock stretches? _____

IC READ TIMING

t_{DA}: Data Access time   30 ns Max

t_{DH}: Data Hold Time   15 ns Min

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