EE 308 – Homework 8

Due March 20, 2006

For all problems below assume your are using a MCS12DP256 chip with a 24 MHz bus clock and an 8 MHz oscillator clock.

1. The table below shows some values in the HCS12's PWM registers:

PWMCAE	PWMCLK	PWMPRCLK	PWMPOL	PWME	PWMSCLA
0x00	0x01	0x35	0xFF	0x0F	0x45
PWMSCLB	PWMPER0	PWMPER1	PWMDTY0	PWMDTY1	PWMCTL
0xA5	0xfa	0xC8	0x80	0xc8	0x00

   (a) What is the period (in seconds) of the pulse width modulated signal generated on PWM channel 0?

   (b) What is the duty cycle (in percent) of the pulse width modulated signal on PWM channel 0?

   (c) What is the period (in seconds) of the pulse width modulated signal generated on PWM channel 1?

   (d) What is the duty cycle (in percent) of the pulse width modulated signal on PWM channel 1?

2. You want to set up PWM channel 2 to generate a pulse width modulated signal with a frequency of 5 kHz and a duty cycle of 40%. How will you set up the HCS12 PWM registers to do this? Indicate which clock mode you will use, and the values of PCKB (and PWMSCLB, if you use clock mode 1).

3. Write some C code to set up PWM channel 2 to generate a pulse width modulated signal with a frequency of 5 kHz and a duty cycle of 40%. Be sure your code does not change the function of any other PWM channel?

4. Write a C program which does the following:

   (a) Set up one of the PWM channels for a frequency of 5 kHz.

   (b) Enable timer subsystem for an overflow rate of at least 25 ms.

   (c) Set up one of the timer channels for Input Capture, with interrupts enabled.

   (d) Write an Input Capture interrupt service routine which latches the time of the rising edge on the timer channel you are using.

   (e) Write an infinite loop which does the following:

      i. Read the state of four DIP switches connected to Port B. Set the PWM duty cycle based on those switches as follows:

PB3:0	Duty Cycle	PB3:0	Duty Cycle
0000	6.25%	1000	56.25%
0001	12.50%	1001	62.50%
0010	18.75%	1010	68.75%
0011	25.00%	1011	75.00%
0100	31.25%	1100	81.25%
0101	37.50%	1101	87.50%
0110	43.75%	1110	93.75%
0111	50.00%	1111	100.00%

Have a table of integer values which gives the duty cycles closest to those listed in the table.

ii. Print out the time difference between the last two input capture edges to the screen.

5. An analog signal has a frequency content that varies from 0 Hz to 3.5 kHz. It is to be sampled at a frequency of 5 kHz. Is this sampling rate sufficient to allow for reconstruction of the signal? Why or why not?

6. A 4 kHz signal to to be sampled with the HCS12 ATD converter system. What sampling frequency should be used? Why?

7. What register is the Sequence Complete Flag (SCF) in? How does the SCF flag get set? How do you clear it?

8. Write some code which will enable the A/D converter, put it into 8-bit mode, and convert the analog inputs on pins PAD0 through PAD7 continuously.

9. Write some code which will enable the A/D converter, put it into 10-bit mode, and convert the analog inputs on pins PAD0 through PAD7 once. Add some code which will wait until the eight conversions are completed.