EE 308

Homework 11 Due April 10, 2006

1. The figures below show some things which might be on the HCS12 bus in normal expanded wide mode. For each figure, indicate if that combinations of signals can occur. If so, explain what the memory cycle does — read or write, 8-bit or 16-bit access, what data is read from or written to, what memory address(es) are accessed. If the combination of signals cannot occur, explain why not.

E			
AD15-0	0x1234	 0x4321	
r/w			
LSTRB	 		
E			
AD15-0	0x2345	0x5432	
R/W			
LSTRB			
E			
AD15-0	0x3456	0x6543	
r/W		 	
LSTRB			
Е —			
AD15-0	0x4567	0x7654	
r/\			
LSTRB			

2. The following table shows some values in the HC12 memory:

	0	1	2	3	4	5	6	7	8	9	A	В	C	D	E	F
4080	01	ЗF	C6	80	5B	86	C6	03	5B	8D	C6	FF	5B	02	4C	80

Show what will be on the address/data bus and the control lines when the HC12 does the following:

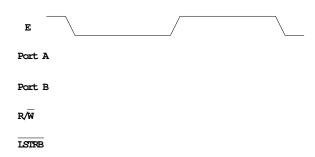
(a) Writes a 0xAA to address 0x4080.



(b) Writes a 0x55AA to the two bytes at addresses 0x4082 and 0x4083.

E		
Port A		
Port B		
R∕₩		
LSTRB		
D 1 · 1 1 · C	11 0 400	0

(c) Reads a single byte from addresses 0x4089.



- 3. Immediately upon coming out of reset, an HCS12 is operating in Normal Expanded Wide mode. How did the HCS12 know it should run in this mode i.e. what pins did it check, and what was the state of those pins?
- 4. Immediately upon coming out of reset, an HCS12 is operating in Normal Single Chip mode. How did the HCS12 know it should run in this mode — i.e. what pins did it check, and what was the state of those pins?
- 5. Immediately upon coming out of reset, an HCS12 is operating in Normal Single Chip mode. How can you switch the chip into Normal Expanded Wide mode? Write some code to do this.

- 6. You want to use an Altera 7064 chip to implement an 8-bit input port at address 0x4000, and an 8-bit output port at address 0x4001. Write an Altera TDF file, or draw an Altera GDF file, which does the following:
 - (a) Demultiplexes the address from the data. It generates the output lines A15-0. The inputs are AD15-0 and the E clock.
 - (b) Does the address decoding:
 - Generates an output R4000 which goes low when the HCS12 does a read from the byte at memory address 0x4000.
 - Generates an output W4001 which goes low when the HCS12 does a write to the byte at memory address 0x4001.
 - Generates an output R4001 which goes low when the HCS12 does a read from the byte at memory address 0x4001.

The inputs to the device should be address lines A15-0, and the E, R/\overline{W} , and \overline{LSTRB} lines.