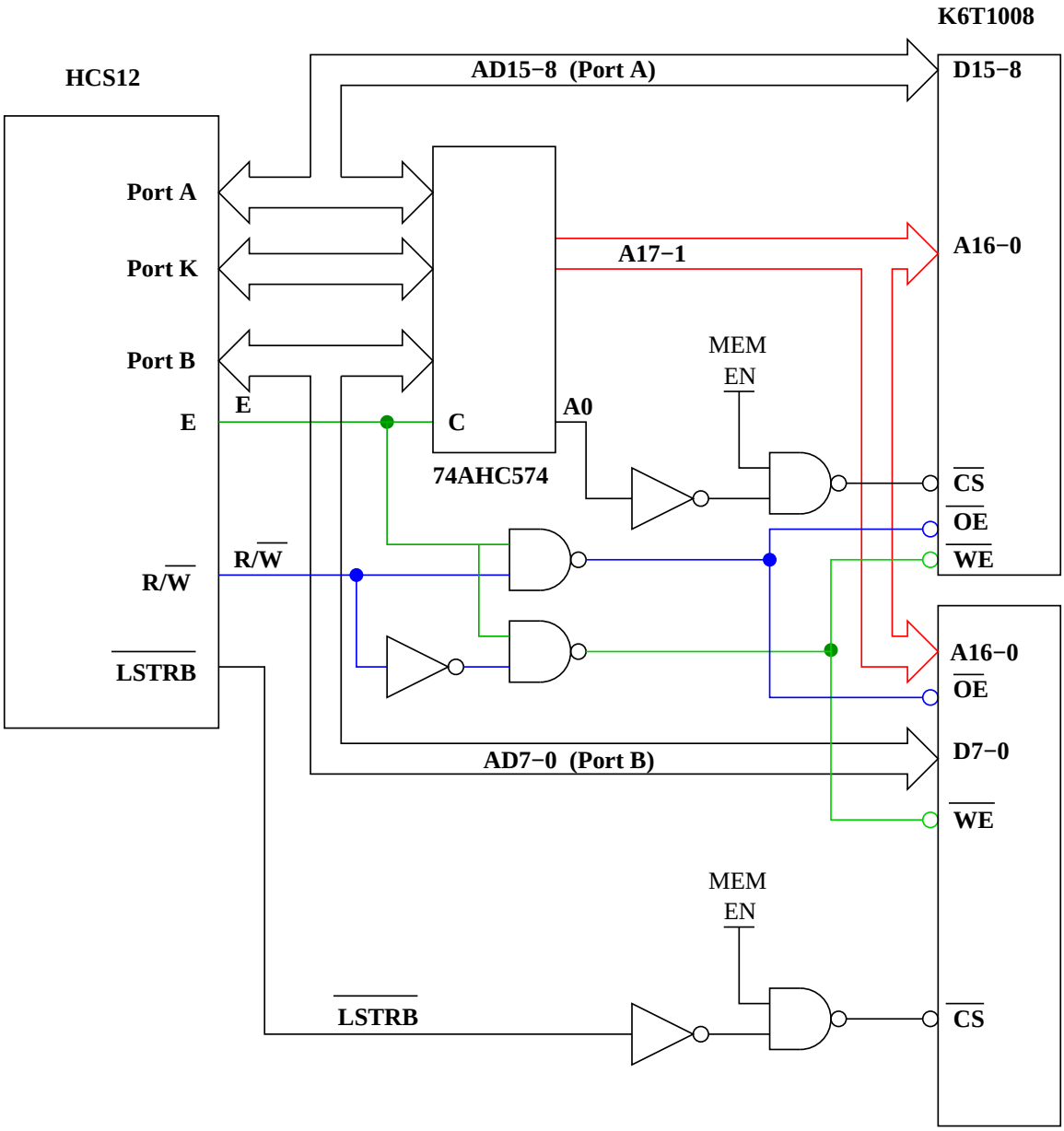
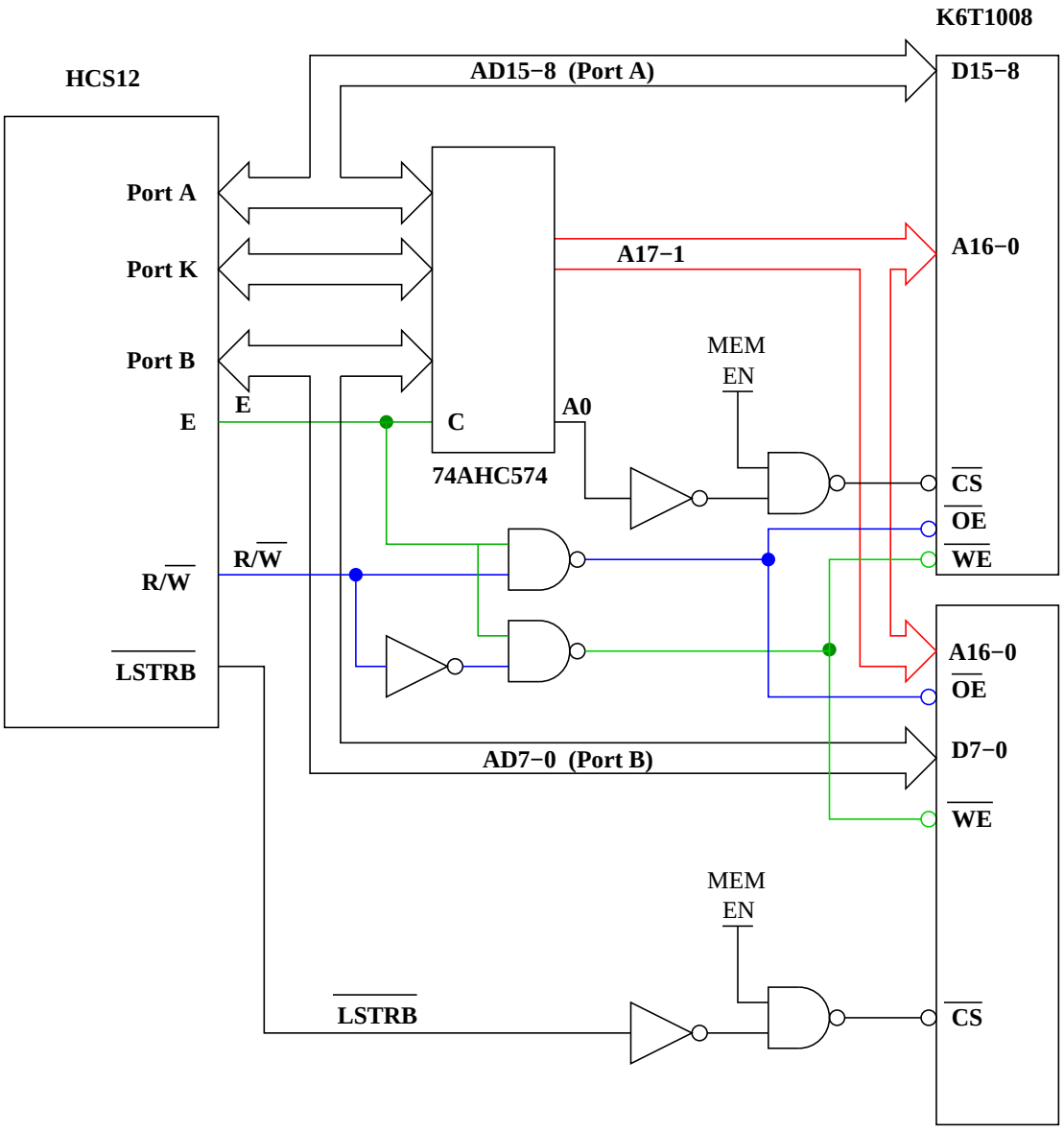
Using the HCS12 Expanded Bus — Timing Issues

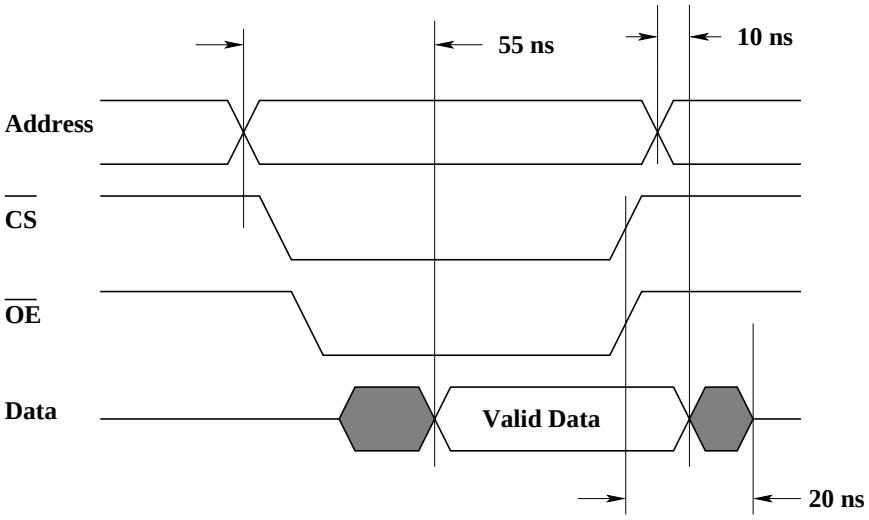
- In expanded mode, memory and peripherals can be added to the HCS12.
- In order for the expansion to work, the interface timing must be correct.
- Here we will discuss adding more RAM memory to the HCS12.
- It is necessary to look at the timing of the HCS12, the "glue logic" (the chips between the HCS12 and the memory) and the memory to see if all the specs are met.
- The HCS12 evaluation board you use in lab has 256 kB of external RAM. We do not use this RAM for two reasons:
  - As you will see below, the external RAM will not work with a 24 MHz bus clock. Because there is plenty of RAM in the HCS12 itself, we disable the external RAM so we can run the HCS12 at 24 MHz.
  - The external RAM is not supported by DBug-12. We could not use DBug-12 if we used the external RAM.
- Below we will analyze the timing issues for the external memory, and find out what frequency of HCS12 bus clock is needed to be able to use the external RAM.
- The RAM used on the evaluation board is a 55 ns Samsung K6T1008C2E

Schematic of Memory Expansion




K6T1008
HCS12
AD15−8 (Port A)
D15−8
Port A
Port K
Port B
E
R/W
LSTRB
A17−1
A16−0
MEM
EN
E
C
A0
74AHC574
CS
OE
WE
R/W
A16−0
OE
D7−0
AD7−0 (Port B)
WE
MEM
EN
LSTRB
CS

READ CYCLE


55 ns
10 ns
Address
CS
OE
Data
Valid Data
20 ns

Bus clock frequency needed for memory expansion

- The control signals for the memory are generated by the HCS12 and the glue logic.
- With a 24 MHz bus clock, the time E-clock is high is about 21 ns.
- The memory chip needs the address stable for 55 ns before it can get the data out of its memory.
- The memory cannot work with an HCS12 using a 24 MHz clock.
- With a 4 MHz oscillator, the HCS12 can use a bus clock of 4 MHz, 8 MHz, 12 MHz, 16 MHz, 20 MHz or 24 MHz.
- To have the address stable for 55 ns, the clock period must be greater than 110 ns, which corresponds to a 9 MHz frequency.
- To have the address stable for 55 ns, the bus clock frequency must be less than 9 MHz. The expansion board uses an 8 MHz bus clock.
- Assume 3 ns for signals to propagate through the glue logic chips.

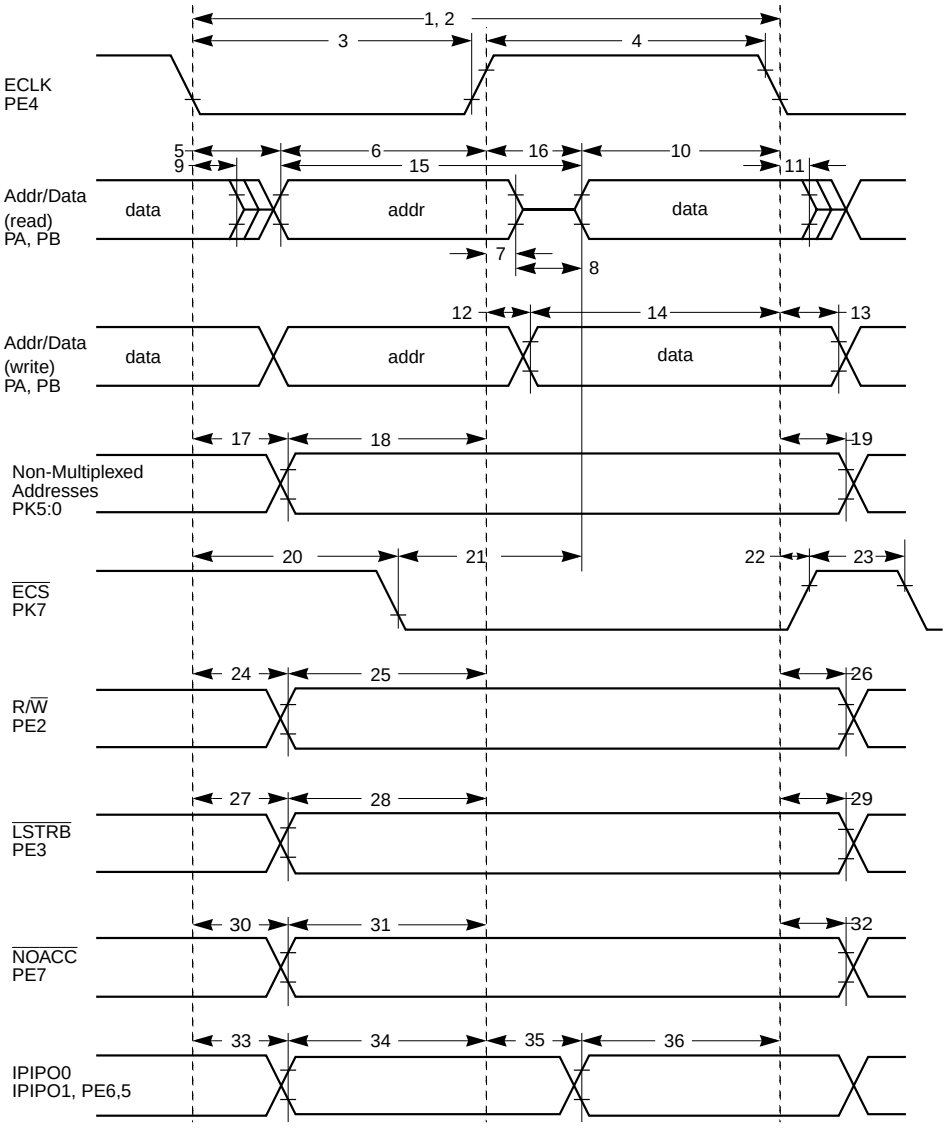


Figure A-9 General External Bus Timing

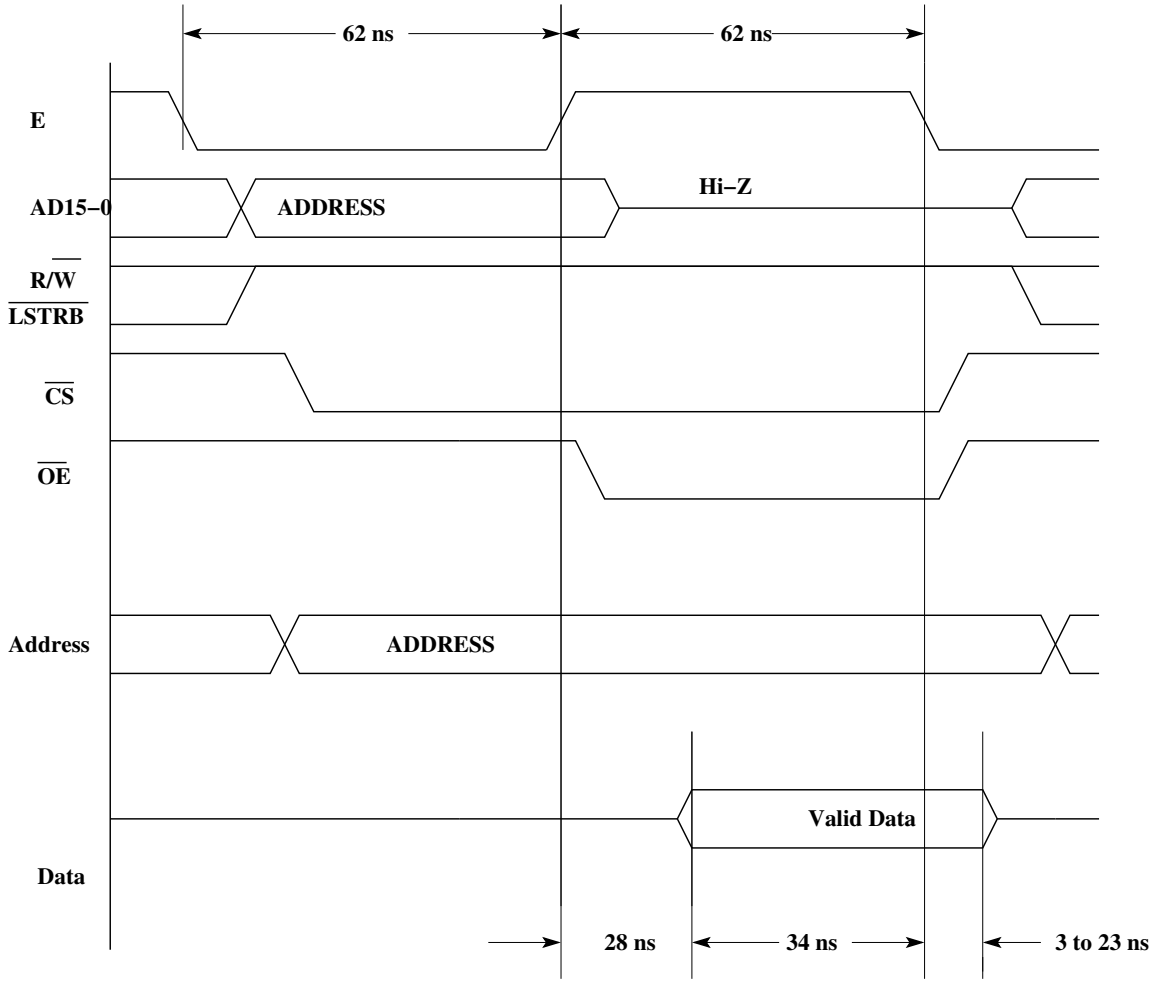
Table A-20 Expanded Bus Timing Characteristics

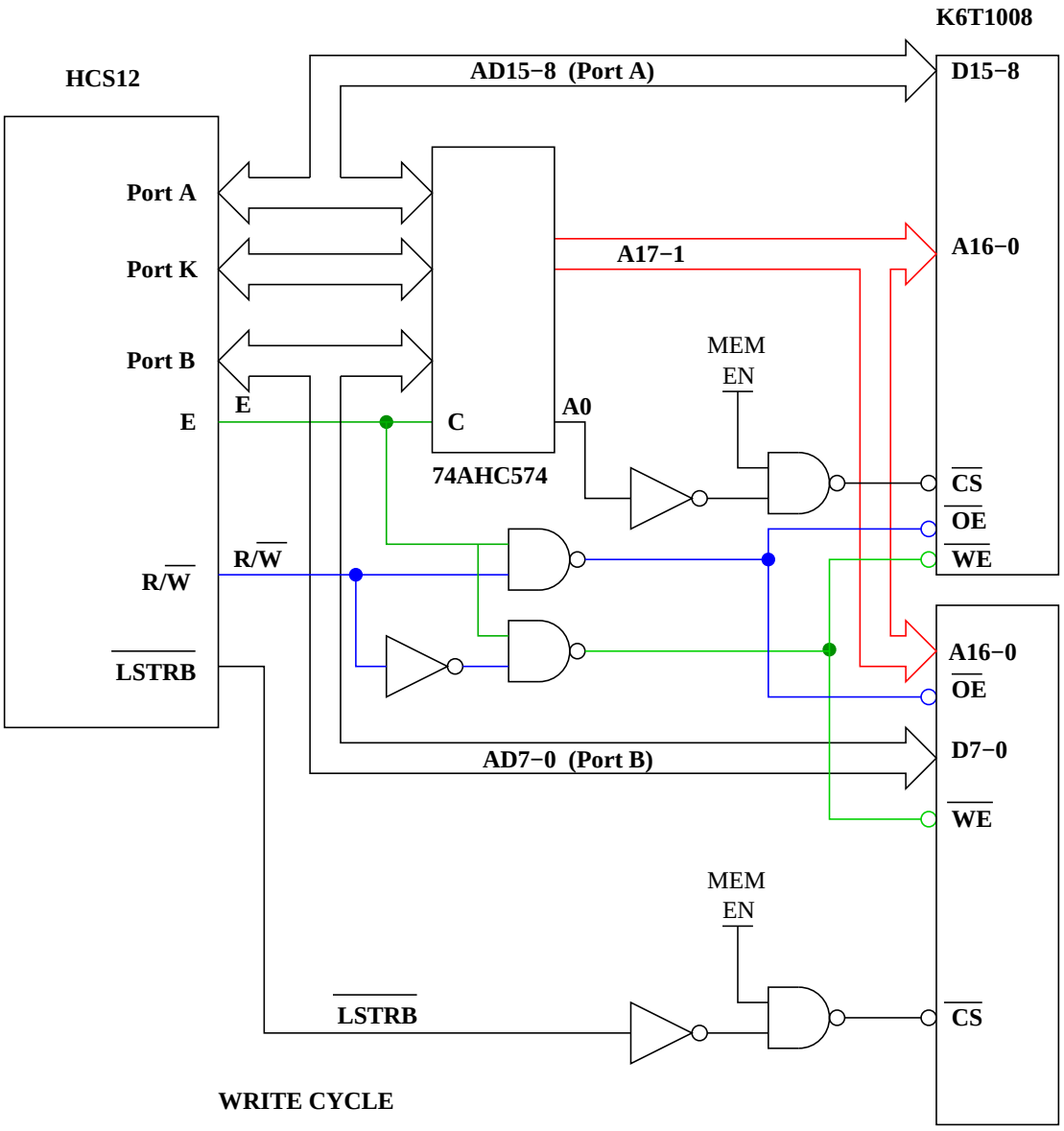
Conditions are shown in **Table A-4** unless otherwise noted, C_{LOAD} = 50pF							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Frequency of operation (E-clock)	f_o	0		25.0	MHz
2	P	Cycle time	t_{cyc}	40			ns
3	D	Pulse width, E low	PW_{EL}	19			ns
4	D	Pulse width, E high[1]	PW_{EH}	19			ns
5	D	Address delay time	t_{AD}			8	ns
6	D	Address valid time to E rise (PW_{EL}–t_{AD})	t_{AV}	11			ns
7	D	Muxed address hold time	t_{MAH}	2			ns
8	D	Address hold to data valid	t_{AHDS}	7			ns
9	D	Data hold to address	t_{DHA}	2			ns
10	D	Read data setup time	t_{DSR}	13			ns
11	D	Read data hold time	t_{DHR}	0			ns
12	D	Write data delay time	t_{DDW}			7	ns
13	D	Write data hold time	t_{DHW}	2			ns
14	D	Write data setup time[1] (PW_{EH}–t_{DDW})	t_{DSW}	12			ns
15	D	Address access time[1] (t_{cyc}–t_{AD}–t_{DSR})	t_{ACCA}	19			ns
16	D	E high access time[1] (PW_{EH}–t_{DSR})	t_{ACCE}	6			ns
17	D	Non-multiplexed address delay time	t_{NAD}			6	ns
18	D	Non-muxed address valid to E rise (PW_{EL}–t_{NAD})	t_{NAV}	15			ns
19	D	Non-multiplexed address hold time	t_{NAH}	2			ns
20	D	Chip select delay time	t_{CSD}			16	ns
21	D	Chip select access time[1] (t_{cyc}–t_{CSD}–t_{DSR})	t_{ACCS}	11			ns
22	D	Chip select hold time	t_{CSH}	2			ns
23	D	Chip select negated time	t_{CSN}	8			ns
24	D	Read/write delay time	t_{RWD}			7	ns
25	D	Read/write valid time to E rise (PW_{EL}–t_{RWD})	t_{RWV}	14			ns
26	D	Read/write hold time	t_{RWH}	2			ns
27	D	Low strobe delay time	t_{LSD}			7	ns
28	D	Low strobe valid time to E rise (PW_{EL}–t_{LSD})	t_{LSV}	14			ns
29	D	Low strobe hold time	t_{LSH}	2			ns
30	D	NOACC strobe delay time	t_{NOD}			7	ns
31	D	NOACC valid time to E rise (PW_{EL}–t_{NOD})	t_{NOV}	14			ns

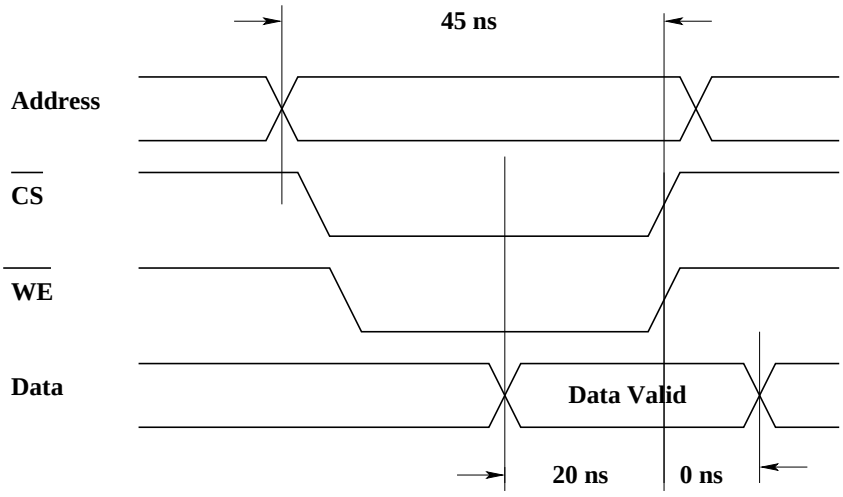
Memory Read

- CS for even memory chip
  1. E goes low
  2. 8 ns later, AD15-0 change into address (HCS12 spec)
  3. 3 ns later, A15-0 comes out of 74AHC573 (glue logic)
  4. 6 ns later, CS goes low for even memory chip. (glue logic)
  5. CS goes low 17 ns after E goes low. (Total)
- CS for odd chip about same; CS for odd chip goes low 14 ns after E goes low
- Output Enable (OE)
  1. E goes high
  2. 3 ns later, OE goes low (glue logic)
  3. OE goes low 3 ns after E goes high (Total)
- Valid Data from Memory
  1. E goes low
  2. 8 ns later, AD15-0 change into address (HCS12)
  3. 3 ns later, A15-0 comes out of 74AHC573 (glue logic)
  4. 55 ns later, valid data is available from memory chip (memory)
  5. 66 ns after E goes low, valid data is available (but not on bus) (Total)
- Data from Memory put onto bus
  1. E goes high
  2. 3 ns later, OE goes low (glue logic)
  3. 25 ns later, memory chip puts data onto bus (memory)
  4. 28 ns after E goes low, data from memory is put onto bus (total)

- HCS12 reads data
  1. HCS12 needs data on bus 13 ns before E goes low (HCS12)
  2. E goes low 62 ns - 28 ns = 34 ns before E goes low (Total)
  3. **This meets the HCS12 data setup time**
- Data removed from bus
  1. HCS12 needs data on bus 0 ns after E goes low (HCS12)
  2. OE goes high 3 ns after E goes low (glue logic)
  3. Data removed from bus 0 to 20 ns after OE goes high (memory)
  4. Data on bus 3 ns to 23 ns after E goes low (Total)
  5. **This meets the HCS12 data hold time**
- **The memory chip will work with the RAM for read cycles**




K6T1008
HCS12
AD15−8 (Port A)
D15−8
Port A
Port K
Port B
E
R/W
LSTRB
E
C
A0
74AHC574
A17−1
A16−0
MEM
EN
CS
OE
WE
R/W
A16−0
OE
D7−0
WE
AD7−0 (Port B)
MEM
EN
LSTRB
CS


WRITE CYCLE
45 ns
Address
CS
WE
Data
Data Valid
20 ns
0 ns

Memory Write

- CS for even memory chip
  1. E goes low
  2. 8 ns later, AD15-0 change into address (HCS12)
  3. 3 ns later, A15-0 comes out of 74AHC573 (glue logic)
  4. 6 ns later, CS goes low for even memory chip. (glue logic)
  5. CS goes low 17 ns after E goes low (Total)
- CS for odd chip about same; CS for odd chip goes low 14 ns after E goes low
- Write Enable (WE)
  1. E goes high
  2. 3 ns later, WE goes low (glue logic)
  3. WE goes low 3 ns after E goes low (Total)
- HCS12 puts data on bus
  1. E goes high
  2. 7 ns later, AD15-0 change into data (HCS12)
  3. 7 ns after E goes high, HCS12 puts data on bus (HCS12)
- Memory latches data
  1. E goes low
  2. 3 ns later, WE goes high (glue logic)
  3. Memory needs data on bus 20 ns before WE goes high (memory)
  4. Data is on bus 58 ns before WE goes high (Total)
  5. **This meets the memory write setup time**

- Data removed from bus
  1. Memory needs data on bus 0 ns after WE goes high (memory)
  2. WE goes high 3 ns after E goes low (glue logic)
  3. Data removed from bus 2 ns after E goes low (HCS12)
  4. Data on bus -1 ns WE goes high (Total)
  5. **Close; will probably meet specs**
- **The memory chip will work with the RAM for write cycles**