Review for Exam 3

A/D Converter

- Power-up A/D converter (ATD1CTL2)
- Write 0x05 to ATD1CTL4 to set at fastest conversion speed and 10-bit conversions
- Write 0x85 to ATD1CTL4 to set at fastest conversion speed and 8-bit conversions
- Select number of conversions in a sequence (ATD1CTL3)
- Select type of conversion sequence and the analog channels sampled (ATD1CTL5)
  - Right/left justified
  - signed/unsigned
  - Continuous Scan vs. Single Scan
  - Multichannel vs. Single Channel conversions
- How to tell when conversion is complete - ATD1STAT0 register
- How to read results of A/D conversions - ATD1DR$[7-0]$H (8-bit left-justified conversions)
- How to read results of A/D conversions - ATD1DR$[7-0]$L (8-bit right-justified conversions)
- How to read results of A/D conversions - ATD1DR$[15-6]$ (10-bit left-justified conversions)
- How to read results of A/D conversions - ATD1DR$[9-0]$ (10-bit right-justified conversions)
  - Be able to convert from digital number to voltage, and from voltage to digital number (need to know V_{RH} and V_{RL}).
- How long does it take to make a conversion?

Serial Communications and the IIC Bus

- Pins used – SDA and SCl
- Difference of use in Master and Slave mode
- IIC serial format for writing to slave
  - Start condition, 7-bit slave address, R/$\overline{\text{W}}$, wait for acknowledge
  - Send eight data bits, wait for ACK, repeat, send stop condition
- IIC serial format for reading from slave
  - Start condition, 7-bit slave address, R/$\overline{\text{W}}$, wait for acknowledge
  - Receive eight data bits, send ACK, repeat, after receiving last byte, send NACK instead of ACK, send stop condition
- IIC IBAD (Bus Address) register
  - Set address when used as slave
  - To use as master, write something like 0x01 (any address not assigned to a slave)
- IIC IBFD (Bus Frequency Divide) Register
  - Set clock speed to match slave
- IIC IBCR (Bus Control Register) Register
  - IBEN — Enable IIC bus
  - IBIE — Enable interrupts
  - MS/$\overline{\text{SL}}$ Switch to master mode
  - TX/$\overline{\text{RX}}$ Switch between transmit and receive
  - TKAK — Send an acknowledge
  - RSTA — Send an restart (didn't discuss)
  - IBSWAI — Specify if IIC clock should operate in WAIT mode (didn't discuss)
- IIC IBSR (Bus Status Register) Register
  - TCF — Transmit Complete Flag
  - IAAS — Did not discuss
  - IBB — Did not discuss
  - IBAL — Did not discuss
  - SRW — Did not discuss
  - IBIF — Interrupt flag. Clear by writing a 1 to this bit.
  - RXAK — Did not discuss
- IIC IBDR (Bus Data Register) Register
  - Write data to this register to send to slave
  - Read data from this register to receive from slave

Interfacing

- Getting into expanded mode — MODA, MODB, MDOC pins or MODE Register
- PEAR Register — enable ECLK, LSTRB, R/W on external pins
- Ports A and B in expanded mode
  - Port A – AD 15-8 (Port A is for data for high byte, even addresses)
  - Port B – AD 7-0 (Port B is for data for low byte, odd addresses)
- E clock
  - Address on AD 15-0 when E low, Data on AD 15-0 when E high
  - Need to latch address on rising edge of E clock
  - On write (output), external device latches data on signal initiated by falling edge of E
  - On read (input), HCS12 latches data on falling edge of E
  - E-clock stretch - MISC register
- R/W Line
- LSTRB line
- Single-byte and two-byte accesses
  - 16-bit access of even address – A0 low, LSTRB low – accesses even and odd bytes
  - 8-bit access of even address – A0 low, LSTRB high – accesses even byte only
  - 8-bit access of odd address – A0 high, LSTRB low – accesses odd byte only
  - A0 high and LSTRB high never occurs on external bus.
- Address Decoding – interfacing using MSI chips
- Timing – Be sure to meet setup and hold times of device receiving data
  - For a write, meet setup and hold of external device
  - For a read, meet setup and hold of HC12
- Timing — Be sure to meet address access time (length of time address needs to be on bus before external device is ready)