EE 308 – Homework 8

Due Mar. 23, 2012

For all problems below assume your are using a MCS12DP256 chip with a 24 MHz bus clock and a 8 MHz oscillator clock.

1. The table below shows some values in the HCS12's PWM registers. Note: All values are in hexadecimal.

PWME	PWMPOL	PWMCLK	PWMPRCLK	PWMCAE	PWMCTL	PWMSCLA	PWMSCLB
2D	FF	03	35	00	00	96	FA
PWMPER0	PWMPER1	PWMPER2	PWMPER3	PWMDTY0	PWMDTY1	PWMDTY2	PWMDTY3
C8	64	32	64	78	2F	1C	5A

   (a) What is the period (in seconds) of the pulse width modulated signal generated on PWM channel 0?

   (b) What is the duty cycle (in percent) of the pulse width modulated signal on PWM channel 0?

   (c) What is the period (in seconds) of the pulse width modulated signal generated on PWM channel 2?

   (d) What is the duty cycle (in percent) of the pulse width modulated signal on PWM channel 2?

2. You want to set up PWM channel 2 to generate a pulse width modulated signal with a frequency of 250 Hz and a duty cycle of 40%. How will you set up the HCS12 PWM registers to do this? Indicate which clock mode you will use, and the values of PCKB (and PWMSCLB, if you use clock mode 1).

3. Write some C code to set up PWM channel 2 to generate a pulse width modulated signal with a frequency of 250 kHz and a duty cycle of 40%. Be sure your code does not change the function of any other PWM channel? (Write C code to write the values you found in Problem 2 to the MC9S12 registers.)

4. Write some C code which does the following:

   (a) Sets up one of the PWM channels for a frequency of 5 kHz.

   (b) Has an infinite loop which reads the state of four DIP switches connected to PTH, and sets the PWM duty cycle based on those switches as follows:

PTH3:0	Duty Cycle	PTH3:0	Duty Cycle
0000	6.25%	1000	56.25%
0001	12.50%	1001	62.50%
0010	18.75%	1010	68.75%
0011	25.00%	1011	75.00%
0100	31.25%	1100	81.25%
0101	37.50%	1101	87.50%
0110	43.75%	1110	93.75%
0111	50.00%	1111	100.00%

   Use a table of integer values which gives the duty cycles closest to those listed in the table.

5. Write some C code to do the following:

   (a) Enable the timer subsystem for an overflow rate of at least 25 ms.

   (b) Set up one of the timer channels for Input Capture, with interrupts enabled.

   (c) Write an Input Capture interrupt service routine which latches the time of the rising edge on the timer channel you are using.

6. An analog signal has a frequency content that varies from 0 Hz to 25 kHz. It is to be sampled at a frequency of 40 kHz. Is this sampling rate sufficient to allow for reconstruction of the signal? Why or why not?

7. An analog signal with a frequency content from 0 Hz to 5 kHz signal to to be sampled with the HCS12 ATD converter system. What minimum sampling frequency should be used? Why?

8. A 10-bit A/D converter has $V_{RL} = 0$ V and $V_{RH} = 2.5$ V. Find the voltage values when the A/D conversion results are 40, 100, 250, 750, and 1,000.

9. What register is the Sequence Complete Flag (SCF) in? How does the SCF flag get set? How do you clear it?

10. Write some code which will enable the A/D converter, put it into 10-bit mode, and convert the analog inputs on pins PAD0 through PAD3 continuously.

11. Write some code which will enable the A/D converter, put it into 8-bit mode, and convert the analog inputs on pins PAD0 through PAD3 once. Add some code which will wait until the four conversions are completed.