Lecture 33

April 18, 2012

Setting Baud Rate to 115,200

Using the MC9S12 Expanded Bus — Timing Issues

Setting Baud Rate to 115,200

For Lab 5, you will need to set the Baud rate of the MC9S12 to 115,200. The MC9S12 needs a Baud clock which is 16 times the Baud rate, so the Baud clock needs to be set to a few percent of $115,200 \times 16 = 1,843,200$. Since the MC9S12 has a 24 MHz bus clock, the clock needs to be divided by 13.021. The closest integer to this is 13, so if the 24 MHz clock is divided by 13, the Baud clock will be 0.16% off, which will work fine.

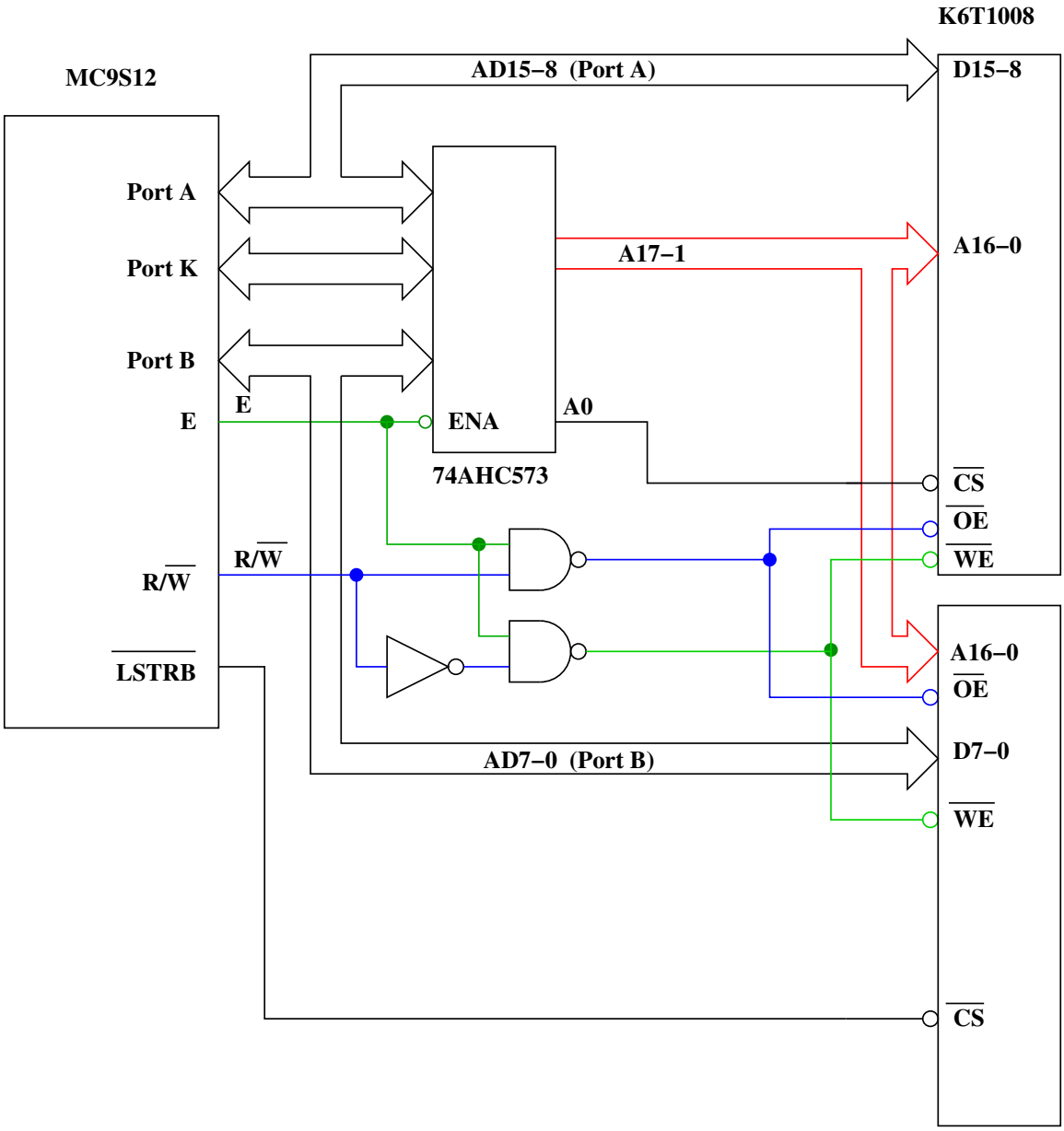
To set the Baud rate to 115,200, you need to write 13 to the 13 bits SBR12 through SBR0. The 5 MSB of SBR are in the SCIBDH register, and the 8 MSB of SBR are in the SCIBDL register. The HyperTerminal is connected to SCI0, so you need to write to the SCI0 registers. You can set the Baud rate to 115,200 with the ollowing commands:

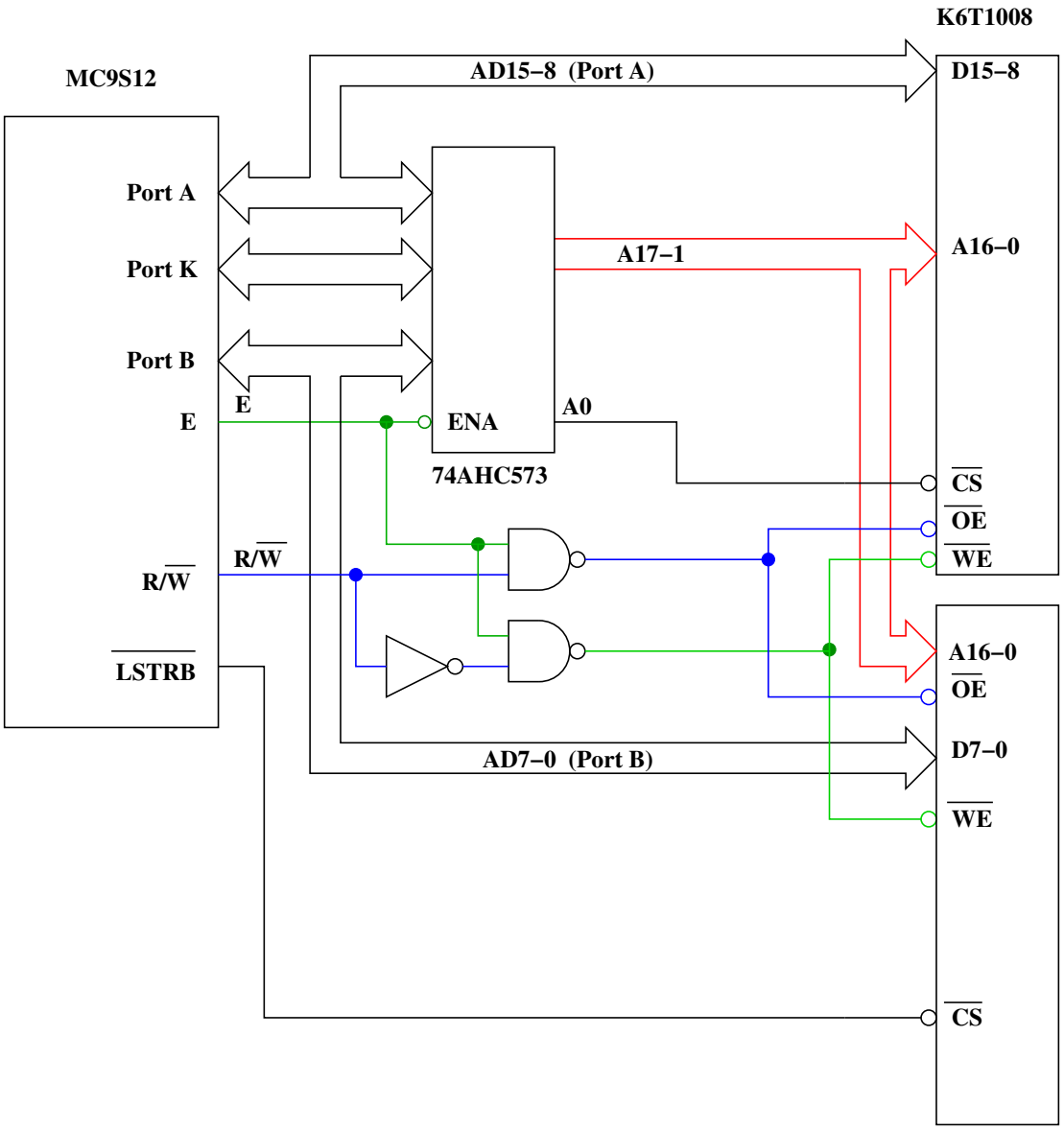
```
SCI0BDH = 0;
SCI0BDL = 13;
```

Using the MC9S12 Expanded Bus — Timing Issues

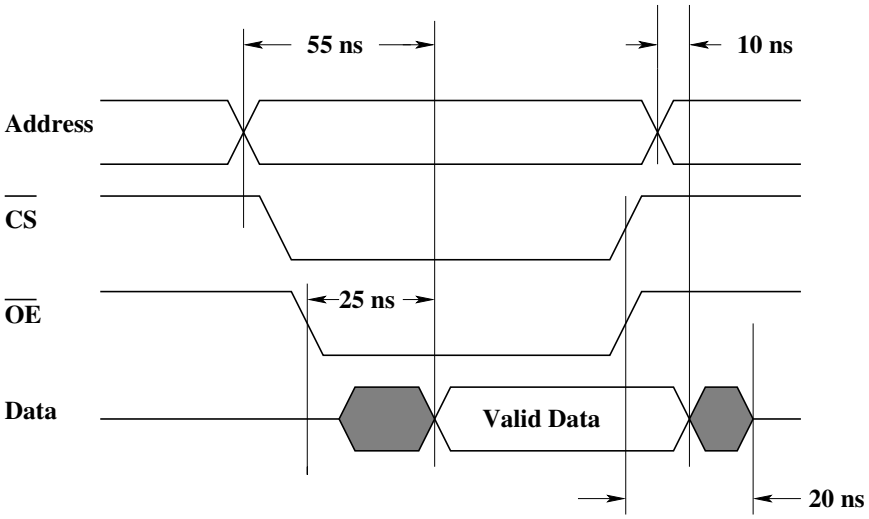
- In expanded mode, memory and peripherals can be added to the MC9S12.
- In order for the expansion to work, the interface timing must be correct.
- Here we will discuss adding more RAM memory to the MC9S12.
- It is necessary to look at the timing of the MC9S12, the "glue logic" (the chips between the MC9S12 and the memory) and the memory to see if all the specs are met.
- Below we will analyze the timing issues for the external memory, and find out what frequency of MC9S12 bus clock is needed to be able to use the external RAM.
- The RAM we will evaluate is a 55 ns Samsung K6T1008C2E
- Note that the interface uses 18 address lines (A17-0). The MC9S12 allows you to use more than 16 address lines by paging the memory. You select a memory page with Port K, and use a CALL and RTC (Return from CALL) instructions to switch pages.
  - The PPAGE register keeps the page value, which is written to Port K.
  - The CALL instruction pushes the 16-bit return address and the current 8-bit page register onto the stack, then loads the address register and page register with new values.
  - The RTC instruction pulls the return address and page register from the stack.

Schematic of Memory Expansion





READ CYCLE (Samsung KST108C2E)



Bus clock frequency needed for memory expansion

- The control signals for the memory are generated by the MC9S12 and the glue logic.
- With a 24 MHz bus clock, the time E-clock is high is about 21 ns.
- The memory chip needs the address stable for 55 ns before it can get the data out of its memory.
- The memory cannot work with an MC9S12 using a 24 MHz clock.
- With an 8 MHz oscillator, the MC9S12 can use a bus clock of 8 MHz, 16 MHz or 24 MHz.
- To have the address stable for 55 ns, the clock period must be greater than 110 ns, which corresponds to a 9 MHz frequency.
- To have the address stable for 55 ns, the bus clock frequency must be less than 9 MHz. The expansion board uses an 8 MHz bus clock.
- With an 8 MHz clock, the clock period is 125 ns. E is high for about 62 ns, and low for about 62 ns.
- Assume 3 ns for signals to propagate through the glue logic chips.

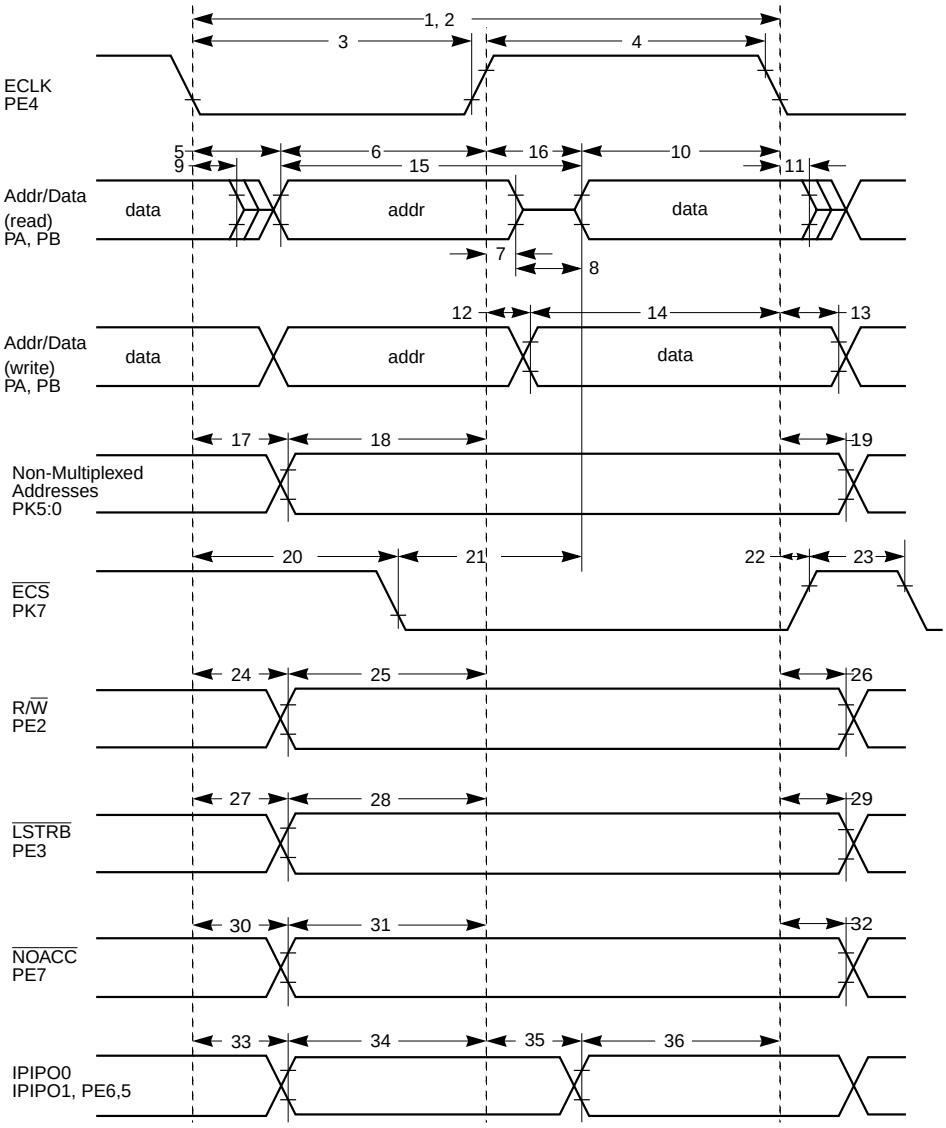


Figure A-9 General External Bus Timing

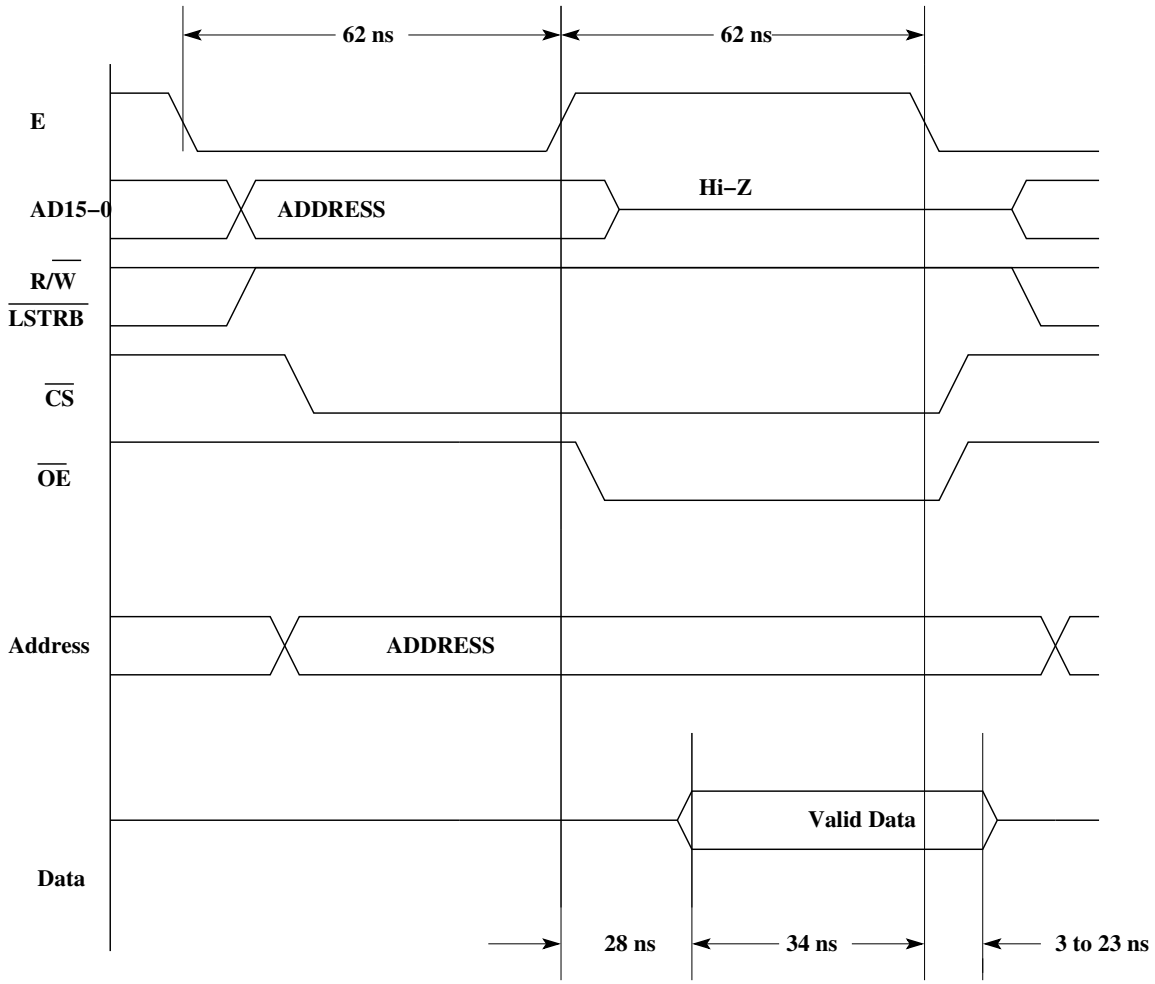
Table A-20 Expanded Bus Timing Characteristics

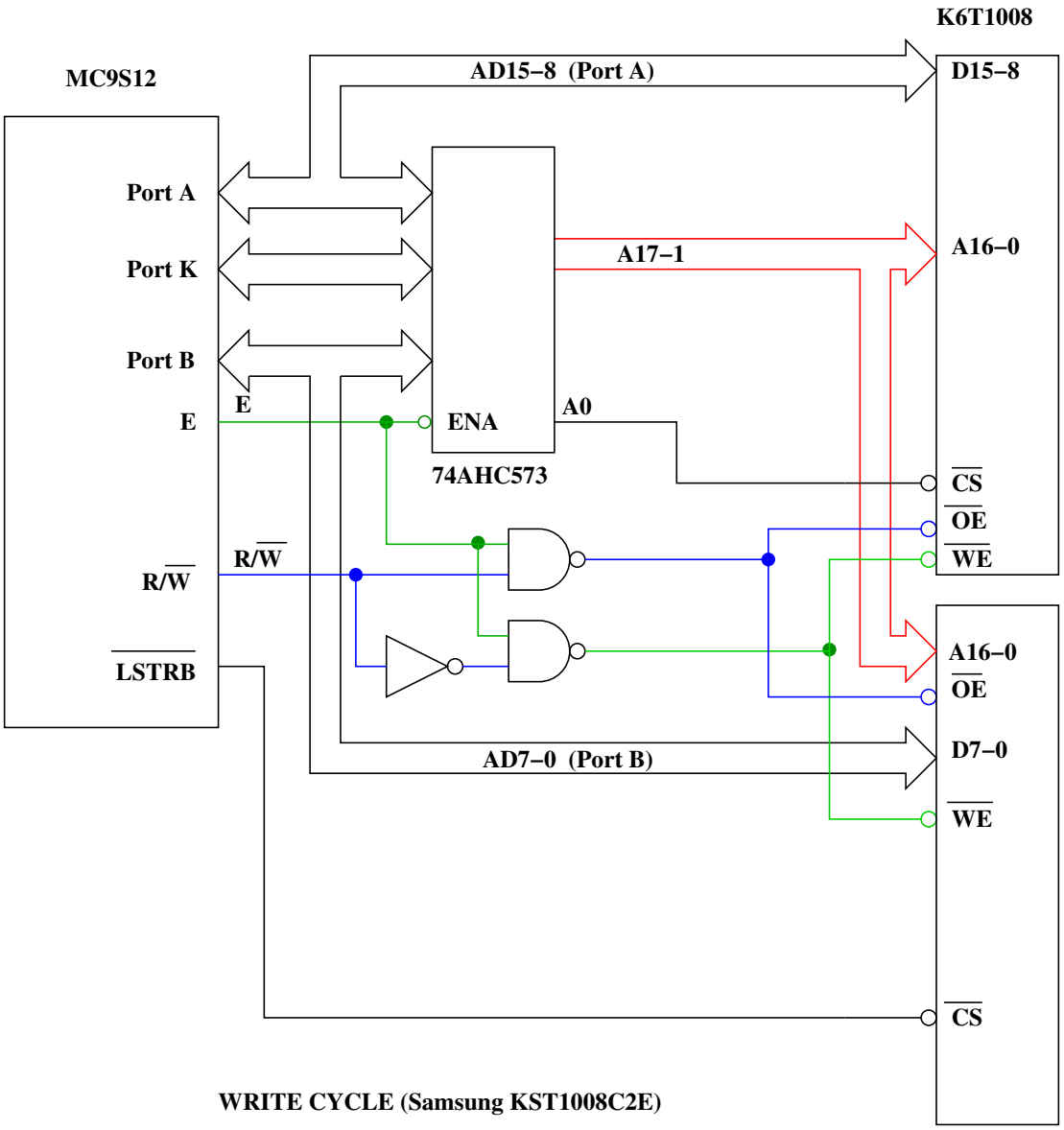
Conditions are shown in **Table A-4** unless otherwise noted, C_{LOAD} = 50pF							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Frequency of operation (E-clock)	f_o	0		25.0	MHz
2	P	Cycle time	t_{cyc}	40			ns
3	D	Pulse width, E low	PW_{EL}	19			ns
4	D	Pulse width, E high[1]	PW_{EH}	19			ns
5	D	Address delay time	t_{AD}			8	ns
6	D	Address valid time to E rise (PW_{EL}–t_{AD})	t_{AV}	11			ns
7	D	Muxed address hold time	t_{MAH}	2			ns
8	D	Address hold to data valid	t_{AHDS}	7			ns
9	D	Data hold to address	t_{DHA}	2			ns
10	D	Read data setup time	t_{DSR}	13			ns
11	D	Read data hold time	t_{DHR}	0			ns
12	D	Write data delay time	t_{DDW}			7	ns
13	D	Write data hold time	t_{DHW}	2			ns
14	D	Write data setup time[1] (PW_{EH}–t_{DDW})	t_{DSW}	12			ns
15	D	Address access time[1] (t_{cyc}–t_{AD}–t_{DSR})	t_{ACCA}	19			ns
16	D	E high access time[1] (PW_{EH}–t_{DSR})	t_{ACCE}	6			ns
17	D	Non-multiplexed address delay time	t_{NAD}			6	ns
18	D	Non-muxed address valid to E rise (PW_{EL}–t_{NAD})	t_{NAV}	15			ns
19	D	Non-multiplexed address hold time	t_{NAH}	2			ns
20	D	Chip select delay time	t_{CSD}			16	ns
21	D	Chip select access time[1] (t_{cyc}–t_{CSD}–t_{DSR})	t_{ACCS}	11			ns
22	D	Chip select hold time	t_{CSH}	2			ns
23	D	Chip select negated time	t_{CSN}	8			ns
24	D	Read/write delay time	t_{RWD}			7	ns
25	D	Read/write valid time to E rise (PW_{EL}–t_{RWD})	t_{RWV}	14			ns
26	D	Read/write hold time	t_{RWH}	2			ns
27	D	Low strobe delay time	t_{LSD}			7	ns
28	D	Low strobe valid time to E rise (PW_{EL}–t_{LSD})	t_{LSV}	14			ns
29	D	Low strobe hold time	t_{LSH}	2			ns
30	D	NOACC strobe delay time	t_{NOD}			7	ns
31	D	NOACC valid time to E rise (PW_{EL}–t_{NOD})	t_{NOV}	14			ns

Memory Read

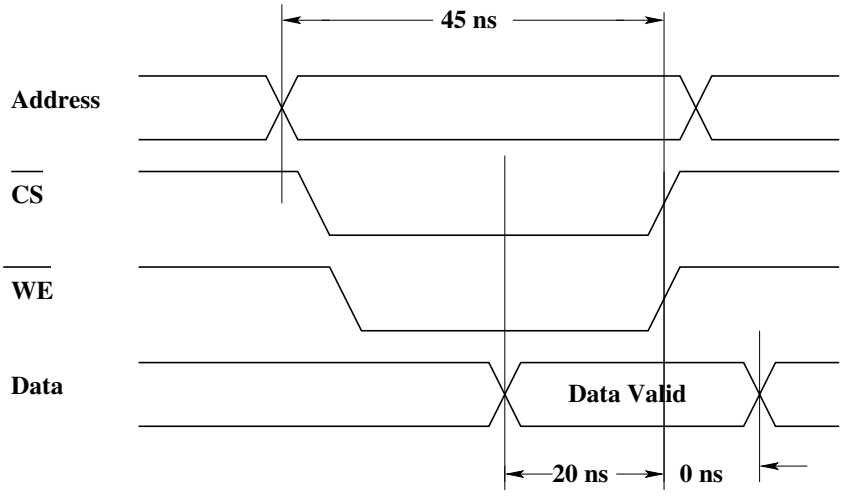
- CS for even memory chip
  1. E goes low
  2. 8 ns later, AD15-0 change into address (MC9S12 spec)
  3. 3 ns later, A15-0 comes out of 74AHC573 (glue logic)
  4. CS goes low 11 ns after E goes low. (Total)
- CS for odd chip is $\overline{\text{LSTRB}}$; CS for odd chip goes low 7 ns after E goes low
- Output Enable (OE)
  1. E goes high
  2. 3 ns later, OE goes low (glue logic)
  3. OE goes low 3 ns after E goes high (Total)
- Valid Data from Memory
  1. E goes low
  2. 8 ns later, AD15-0 change into address (MC9S12)
  3. 3 ns later, A15-0 comes out of 74AHC573 (glue logic)
  4. 55 ns later, valid data is available from memory chip (memory)
  5. 66 ns after E goes low, valid data is available (but not on bus) (Total)
- Data from Memory put onto bus
  1. E goes high
  2. 3 ns later, OE goes low (glue logic)
  3. 25 ns later, memory chip puts data onto bus (memory)
  4. 28 ns after E goes low, data from memory is put onto bus (total)

- MC9S12 reads data
  1. MC9S12 needs data on bus 13 ns before E goes low (MC9S12)
  2. E goes low 62 ns - 28 ns = 34 ns before E goes low (Total)
  3. **This meets the MC9S12 data setup time**
- Data removed from bus
  1. MC9S12 needs data on bus 0 ns after E goes low (MC9S12)
  2. OE goes high 3 ns after E goes low (glue logic)
  3. Data removed from bus 0 to 20 ns after OE goes high (memory)
  4. Data on bus 3 ns to 23 ns after E goes low (Total)
  5. **This meets the MC9S12 data hold time**
- **The memory chip will work with the RAM for read cycles when the MC9S12 uses an 8 MHz bus clock**





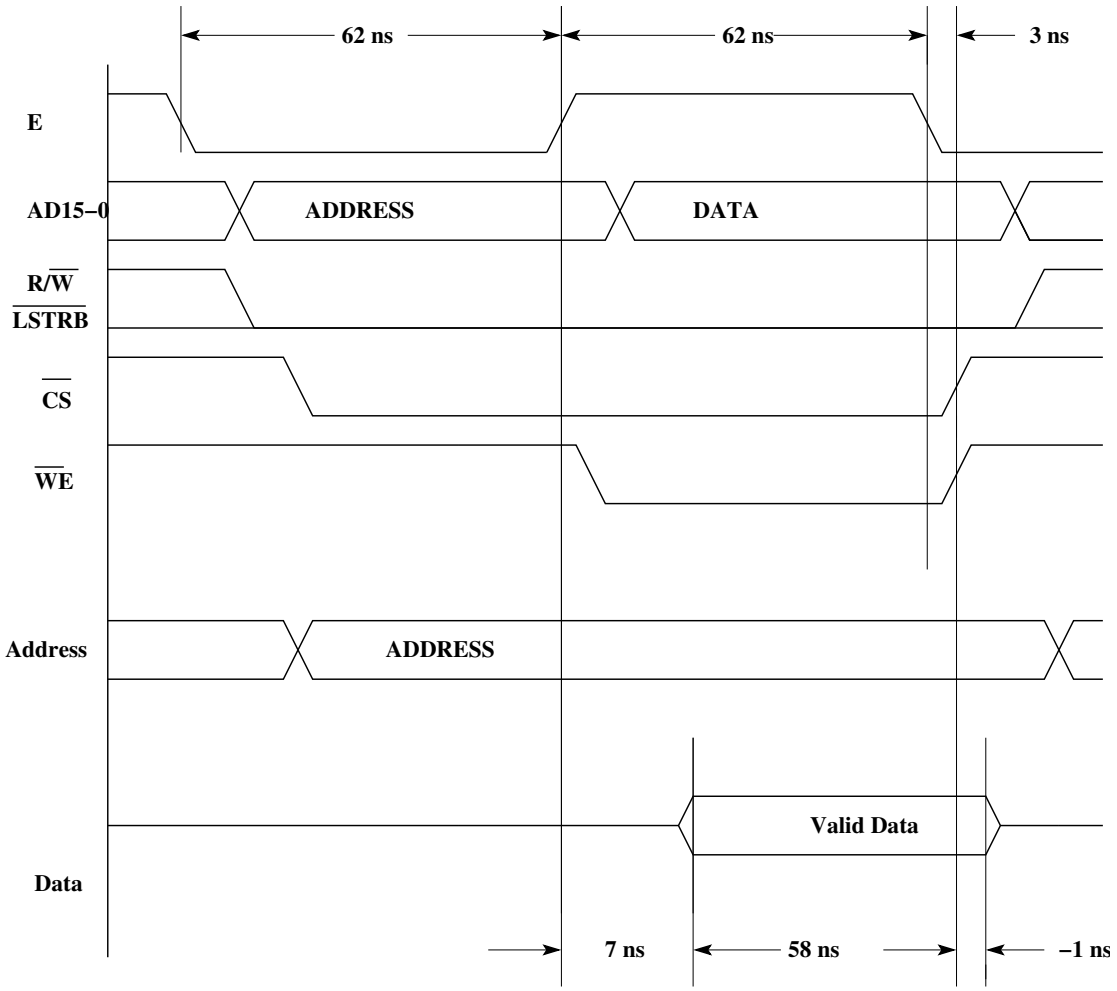
WRITE CYCLE (Samsung KST1008C2E)



Memory Write

- CS for even memory chip. CS for even memory chip is A0.
    1. E goes low
    2. 8 ns later, AD15-0 change into address (MC9S12)
    3. 3 ns later, A15-0 comes out of 74AHC573 (glue logic)
    4. CS goes low 11 ns after E goes low (Total)
- CS for odd chip is $\overline{\text{LSTRB}}$; CS for odd chip goes low 7 ns after E goes low
- Write Enable (WE)
    1. E goes high
    2. 3 ns later, WE goes low (glue logic)
    3. WE goes low 3 ns after E goes low (Total)
- MC9S12 puts data on bus
    1. E goes high
    2. 7 ns later, AD15-0 change into data (MC9S12)
    3. 7 ns after E goes high, MC9S12 puts data on bus (MC9S12)
- Memory latches data
    1. E goes low
    2. 3 ns later, WE goes high (glue logic)
    3. Memory needs data on bus 20 ns before WE goes high (memory)
    4. Data is on bus 58 ns before WE goes high (Total)
    5. **This meets the memory write setup time**

- Data removed from bus
  1. Memory needs data on bus 0 ns after WE goes high (memory)
  2. WE goes high 3 ns after E goes low (glue logic)
  3. Data removed from bus 2 ns after E goes low (MC9S12)
  4. Data on bus -1 ns WE goes high (Total)
  5. **Close; will probably meet specs**
- **The memory chip will work with the RAM for write cycles**



A Faster Memory Chip

- Access time of a memory chip is usually the amount of time from when the chip is selected to the data being available
- For a MC9S12 with a 24 MHz clock, time from address available to time MC9S12 needs data to be ready is [6] + [4], or 11 ns + 19 ns = 30 ns. It will take a few nanoseconds for the glue logic to latch the address, and determine if the chip should be selected. For the circuit shown, there are two propagation delays between a new address available and the chip being selected, so if this is 6 ns, the access time of the memory chip must be less than 30 ns - 6 ns = 24 ns.
- A 12 ns memory chip would probably work for interfacing to the MC9S12 with a 24 MHz bus clock.