EE321 – Lab 10

MOS Field Effect Transistors (MOSFET's), Part I

The purpose of this lab is to investigate the characteristics of MOSFET's, and to use them in some simple circuits. For simplicity we will use only n-channel devices.

Static Characteristics

1. The CMOS CD4007 integrated circuit contains six enhancement MOSFET's, three n-channel and three p-channel. (See the CD4007 datasheet. for its specs.) The n-channel bodies (p-silicon) are connected to pin 7 and must be kept at the most negative voltage used in the circuit. The p-channel bodies (n-silicon) are connected to pin 14 and must be kept at the most positive voltage used in the circuit. The drain and source are interchangeable on Q2 and Q5.

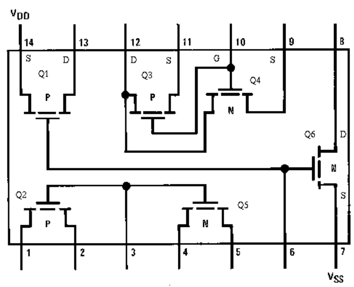

Figure 1.

- WARNING! Although there are protection diodes connected to the input pins to minimize damage from static charge, **Two outputs are not protected. Anti-static precautions must be taken.** Be very careful. Use wrist strap when handling and inserting into the board. Make sure all connections are correct before turning on the power. Ground all unused inputs. Keep your chip in the static bag when not in use. Do not change connections with power on. Connect pins 7 and 14 to the correct voltages.
- Build the circuit in Figure 2 and set the inputs to measure i_D and v_{DS} in the saturation region for one of the n-channel devices (Q5, pins 3, 4, 5) using the circuit shown. With the gate voltage set to about 5 V, adjust the signal generator to a triangle wave with maximum amplitude at 1 kHZ. Be sure to connect pin 7 to ground and pin 14 to +15 V. i_D is proportional to the negative of the voltage across the 100 Ω resistor, ch 2 inverted. Now increase the gate voltage until current is flowing in the MOSFET.

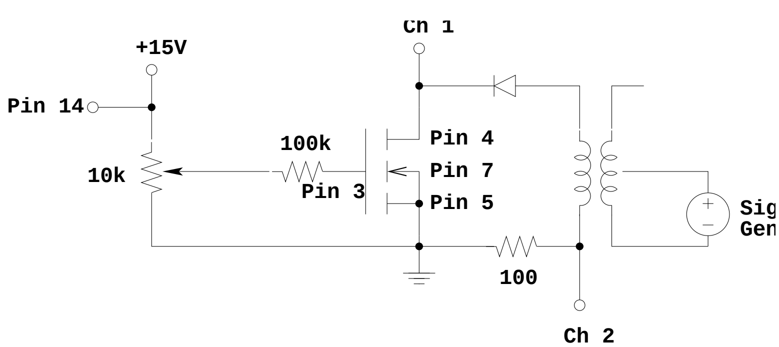

Figure 2.

- Display i_D vs. v_{DS} for the n-Channel FET. Measure V_t by varying the gate voltage until current just begins to flow in the drain circuit (increase the sensitivity of the scope to get a good measurement). Carefully draw the characteristics for one of the transistors at four values of v_{GS}. **Label** your axes.
- Find $k_n'W/L$ from each these curves in the saturation region. If the value of $k_n'W/L$ is much different for each of these v_{GS}, measure V_t again, more carefully.

2. Does the MOSFET behave as a variable resistor for small drain-source voltages (both positive and negative v_{DS})?

   - Find the resistance (from your measurements of the slope with average $v_{DS} = 0$ i.e. no offset) of the MOSFET for small v_{DS} values when $v_{GS} = V_t + 1$. Compare with theory (Sedra and Smith eq. 5.13).
   - Find the resistance for $v_{GS} = 0$ V and 15 V.

Voltage Controlled Switch

3. Construct the "chopper" circuit of Figure 3, which uses a square wave across the gate-source to turn the MOSFET on and off. The path from the drain to source acts as a resistor in a simple voltage divider. The resistance is very high for off and low for on.

   - Note that pin 7 must be connected to -5 V so that v_i can go negative.
   - Set v_i to a 2V p-p sin at 1 kHz and vchop to a square wave from -10 to +10 V at 100 Hz. Sketch or copy the output.
   - Change v_{chop} to 10 kHz and sketch or copy the output.

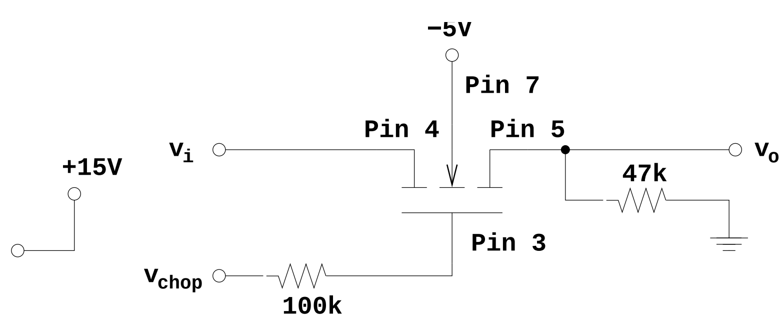

Figure 3.

Variable Gain Amplifier

4. The gain of an op-amp amplifier circuit can be controlled by using a MOSFET as a variable gain-setting resistor. The resistance of the MOSFET can be varied by changing the gate voltage on the FET. Construct the circuit in Figure 4 and apply a small input voltage (less than 50 mV p-p) at 1 kHz. How much can the gain be varied, and does this agree with the range of resistance values for the FET?

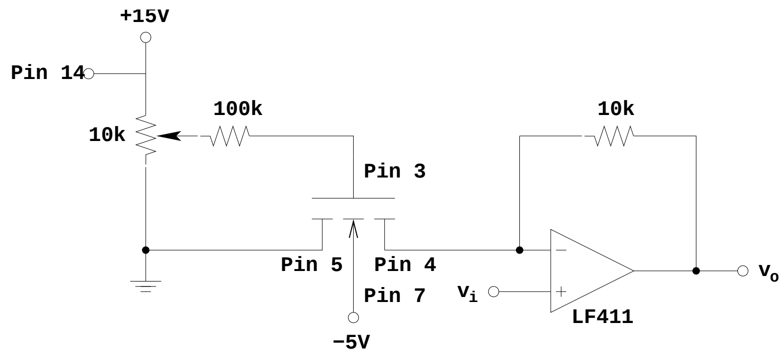

Figure 4.

5. With the gain of the amplifier at approximately 5, increase the input signal amplitude until the output distorts noticeably. What causes the distortion? Sketch a distorted waveform.

6. The distortion can be reduced dramatically by feeding half of the drain voltage back to the gate with R_f, as shown in Figure 5. Connect a 1 V p-p sine wave as shown to vary the gate voltage. The amplifier output should be an amplitude modulated signal.

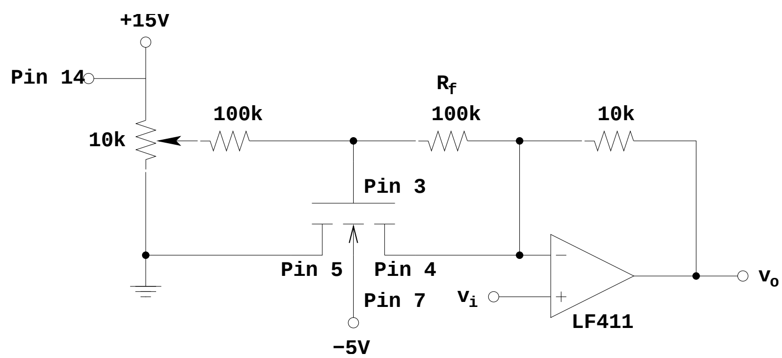

Figure 5.

Pre-Lab

1. What is the purpose of the diode in Figure 1?
2. If V_t is known, how would you find $k_n' W/L$ from the measurement of the drain current in saturation?
3. Write an equation to find V_t and $k_n' W/L$ from the measurement of the drain current (saturated) at two different gate voltages.
4. Find the output v_o of the circuit in Figure 4 as a function of v_i and v_{GS}. Show that, if v_i is small, the output depends only of v_i.
5. Find the output v_o of the circuit in Figure 5 as a function of v_i and v_{GS}.