EE321 – Lab 8

MOS Field Effect Transistors (MOSFET's), Part I

The purpose of this lab is to investigate the characteristics of MOSFET's, and to use them in some simple circuits. For simplicity we will use only n-channel devices.

Static Characteristics

1. The CMOS CD4007 integrated circuit contains six enhancement MOSFET's, three n-channel and three p-channel. (See the CD4007 datasheet. for its specs.) The n-channel bodies (p-silicon) are connected to pin 7 and must be kept at the most negative voltage used in the circuit. The p-channel bodies (n-silicon) are connected to pin 14 and must be kept at the most positive voltage used in the circuit. The drain and source are interchangeable on Q2 (p-channel MOSFET, pins 1, 2 and 3) and Q5 (n-channel MOSFET, pins 4, 5 and 3).

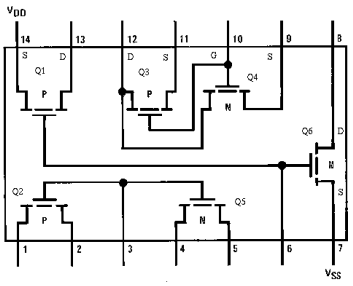

Figure 1.

- WARNING! Although there are protection diodes connected to the input pins to minimize damage from static charge, **Two outputs are not protected. Anti-static precautions must be taken.** Be very careful. Use wrist strap when handling and inserting into the board. Make sure all connections are correct before turning on the power. Ground all unused inputs. Keep your chip in the static bag when not in use. Do not change connections with power on. Connect pins 7 and 14 to the correct voltages.
- In this lab we will use a different method to isolate a signal from ground. In another lab we used an isolation transformer to "float" the signal generator. This creates a potential for a dangerous condition since the case of the signal generator is not grounded. If connected properly and with properly working equipment there is not a danger. In this lab we will use a small signal transformer to isolate the ground of the signal while keeping the case of the signal generator grounded and safe. The primary, P, side of the transformer should be connected to the signal generator (if there is a center tap it should be used to increase the output level).
- Build the circuit in Figure 2 and set the inputs to measure i_D and v_{DS} in the saturation region for one of the n-channel devices (Q5, pins 3, 4, 5) using the circuit shown. With the gate voltage set to about 5 V, adjust the signal generator to a triangle wave with maximum amplitude at 1 kHZ. Be sure to connect pin 7 to ground and pin 14 to +15 V. i_D is proportional to the negative of the voltage across the 100 Ω resistor, ch 2 inverted. Ch 1 is v_{DS}. Now change the gate voltage to control current flowing in the MOSFET.

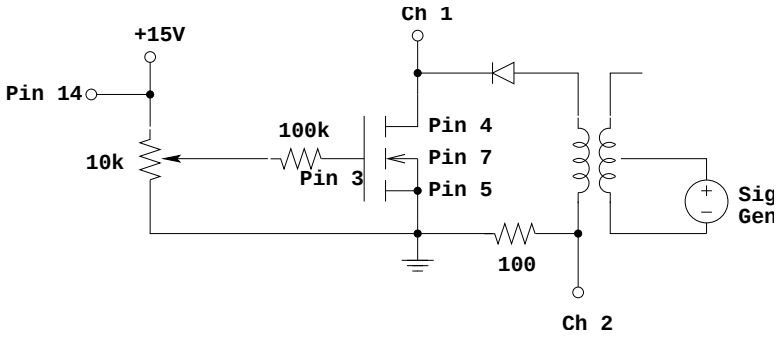

Figure 2.

- Display i_D vs. v_{DS} for the n-Channel FET. The curves should be similar to the curves in Sedra and Smith Figure 4.16.
- Measure V_t by varying the gate voltage until current just begins to flow in the drain circuit (increase the sensitivity of the scope to get a good measurement).
- Carefully draw the characteristics this transistors at four values of v_{GS}. **Label** your axes. One axis should be i_D in mA.
- Find $k_n' W/L$ from one these curves in the saturation region.

2. The MOSFET behave as a variable resistor for SMALL drain-source voltages (both positive and negative v_{DS}) See Figure 4.4 in Sedra and Smith.

   - Decrease the signal amplitude.
   - Find the resistance (from your measurements of the slope with average $v_{DS} = 0$ i.e. no offset) of the MOSFET for small v_{DS} values when $v_{GS} = V_t + 1$. Compare with theory (Sedra and Smith eq. 4.13).
   - Find the resistance for $v_{GS} = 0$ V and 15 V.

Voltage Controlled Switch

3. Construct the "chopper" circuit of Figure 3, which uses a square wave across the gate-source to turn the MOSFET on and off. The path from the drain to source acts as a resistor in a simple voltage divider. The resistance is very high for off and low for on.

   - Note that pin 7 must be connected to -5 V so that v_i can go negative.
   - Set v_i to a 2V p-p sin at 1 kHz and v_{chop} to a square wave from -10 to +10 V at 100 Hz. Sketch or copy the output.
   - Change v_{chop} to 10 kHz and sketch or copy the output.

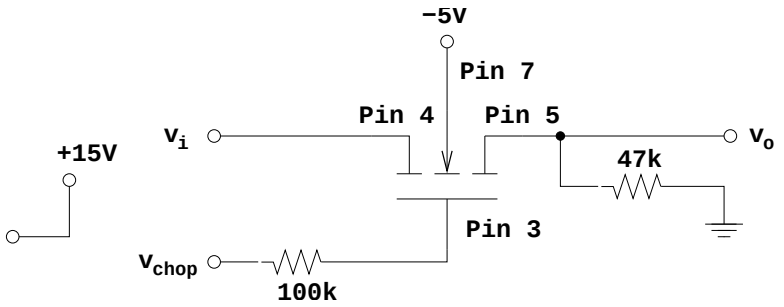

Figure 3.

Variable Gain Amplifier

4. The gain of an op-amp amplifier circuit can be controlled by using a MOSFET as a variable gain-setting resistor. The resistance of the MOSFET can be varied by changing the gate voltage on the FET. Construct the circuit in Figure 4 and apply a small input voltage (less than 50 mV p-p) at 1 kHz. How much can the gain be varied, and does this agree with the range of resistance values for the FET?

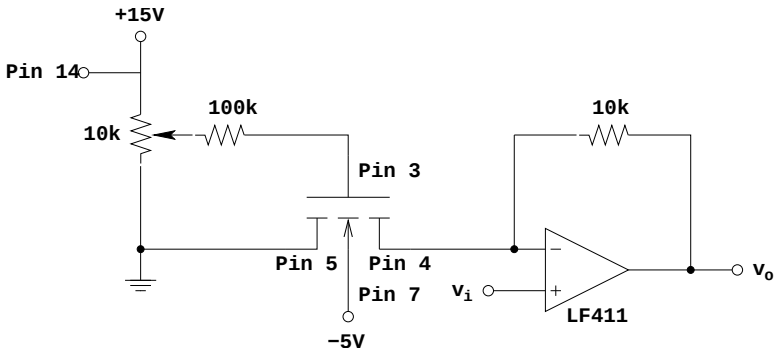

Figure 4.

5. With the gain of the amplifier at approximately 5, increase the input signal amplitude until the output distorts noticeably. What causes the distortion? Sketch a distorted waveform.

6. The distortion can be reduced dramatically by feeding half of the drain voltage back to the gate with R_f, as shown in Figure 5. Connect a 1 V p-p sine wave as shown to vary the gate voltage. Increase the input signal amplitude until the output distorts noticeably. Is there an improvement?

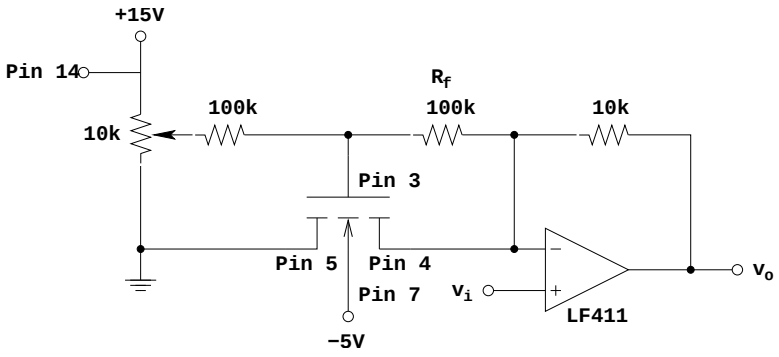

Figure 5.

Pre-Lab

1. What is the purpose of the diode in Figure 2? OR Why don't we want a negative voltage at pin 4?

2. If V_t is known, how would you find $k'_n W/L$ from the measurement of the drain current in saturation?

3. Find the output v_o of the circuit in Figure 4 as a function of v_i and v_{GS}. Assume the FET is in the triode region and its current is determined by v_{GS} and v_{DS}. That current will determine v_o. Show that, if v_i is small, the output depends only of v_i.

4. Find the output v_o of the circuit in Figure 5 as a function of v_i and v_{GS}.