**QUADRATURE CLOCK CONVERTER**

**FEATURES:**
- X1 and X4 mode selection
- Up to 16 MHz output clock frequency
- Programmable output clock pulse width
- On-chip filtering of inputs for optical or magnetic encoder applications.
- TTL and CMOS compatible I/Os
- +4.75V to +10.5V operation (V_{DD}-V_{SS})
- 8-Pin DIP (SOIC available)

**DESCRIPTION:**
The LS7083 and LS7084 are monolithic CMOS silicon gate quadrature clock converters. Quadrature clocks derived from optical or magnetic encoders, when applied to the A and B inputs of the LS7083/LS7084, are converted to strings of Up Clocks and Down Clocks (LS7083) or a Clock and an Up/Down direction control (LS7084). These outputs can be interfaced directly with standard Up/Down counters for direction and position sensing of the encoder.

**INPUT/OUTPUT DESCRIPTION:**

**RBIAS (Pin 1)**
Input for external component connection. A resistor connected between this input and V_{SS} adjusts the output clock pulse width (T_{OW}). For proper operation, the output clock pulse width must be less than or equal to the A,B pulse separation (T_{OW}≤T_{PS}).

**V_{DD} (Pin 2)**
Supply Voltage positive terminal.

**V_{SS} (Pin 3)**
Supply Voltage negative terminal.

**A (Pin 4)**
Quadrature Clock Input A. This input has a filter circuit to validate input logic level and eliminate encoder dither.

**B (Pin 5)**
Quadrature Clock Input B. This input has a filter circuit identical to input A.

**X4/X1 (Pin 6)**
This input selects between X1 and X4 modes of operation. A high-level selects X4 mode and a low-level selects the X1 mode. In X4 mode, an output pulse is generated for every transition at either A or B input. In X1 mode, an output pulse is generated in one combined A/B input cycle. (See Figure 2.)

**LS7083 - DNCK (Pin 7)**
In LS7083, this is the DOWN Clock Output. This output consists of low-going pulses generated when A input lags the B input.

**LS7084 - UP/DN (Pin 7)**
In LS7084, this is the count direction indication output. When A input leads the B input, the UP/DN output goes high indicating that the count direction is UP. When A input lags the B input, UP/DN output goes low, indicating that the count direction is DOWN.

**LS7083 - UPCK (Pin 8)**
In LS7083, this is the UP Clock output. This output consists of low-going pulses generated when A input leads the B input.

**LS7084 - CLK (Pin 8)**
In LS7084, this is the combined UP Clock and DOWN Clock output. The count direction at any instant is indicated by the UP/DN output (Pin7).

**NOTE:** For the LS7084, the timing of CLK and UP/DN requires that the counter interfacing with LS7084 counts on the rising edge of the CLK pulses.
### ABSOLUTE MAXIMUM RATINGS:

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>VALUE</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Supply Voltage</td>
<td>VDD - VSS</td>
<td>12</td>
<td>V</td>
</tr>
<tr>
<td>Voltage at any input</td>
<td>VIN</td>
<td>VSS - .3 to VDD + .3</td>
<td>V</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>TA</td>
<td>0 to +70</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>TSTG</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

### DC ELECTRICAL CHARACTERISTICS:
(All voltages referenced to VSS, TA = 0°C to 70°C.)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>CONDITION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>VDD</td>
<td>4.75</td>
<td>10.5</td>
<td>V</td>
<td>VDD = 10.5V, All ( R_{BIAS} = 2M\Omega )</td>
</tr>
<tr>
<td>Supply current</td>
<td>IDD</td>
<td>-</td>
<td>6.0</td>
<td>µA</td>
<td>( VDD = 10.5V ) ( \text{All} ) ( f_{VDD} = 0 \text{Hz} ) ( R_{BIAS} = 2M\Omega )</td>
</tr>
</tbody>
</table>

### X4/X1 Logic Low

- \( \text{VIL} \) \( - \) \( 0.3V_{DD} \) \( V \) |

### A,B Logic Low

- \( \text{VIL} \) \( - \) \( 0.6 \) \( V \) \( VDD = 4.75V \) |
- \( \text{VIL} \) \( - \) \( 1.0 \) \( V \) \( VDD = 9V \) |
- \( \text{VIL} \) \( - \) \( 1.1 \) \( V \) \( VDD = 10.5V \) |

### X4/X1 Logic High

- \( \text{VIH} \) \( 0.7V_{DD} \) \( - \) \( V \) |

### A,B Logic High

- \( \text{VIH} \) \( 3.1 \) \( - \) \( V \) \( VDD = 4.75V \) |
- \( \text{VIH} \) \( 5.0 \) \( - \) \( V \) \( VDD = 9V \) |
- \( \text{VIH} \) \( 5.6 \) \( - \) \( V \) \( VDD = 10.5V \) |

### ALL OUTPUTS:

Sink Current

- \( \text{IOL} \) \( 1.75 \) \( - \) \( mA \) \( VDD = 4.75V \) |
- \( \text{IOL} \) \( 5.0 \) \( - \) \( mA \) \( VDD = 9V \) |
- \( \text{IOL} \) \( 5.7 \) \( - \) \( mA \) \( VDD = 10.5V \) |

Source Current

- \( \text{IOH} \) \( 1.0 \) \( - \) \( mA \) \( VDD = 4.75V \) |
- \( \text{IOH} \) \( 2.5 \) \( - \) \( mA \) \( VDD = 9V \) |

### TRANSIENT CHARACTERISTICS:
(TA = 0°C to 70°C)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>CONDITION</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \text{A,B} ) inputs:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Validation Delay</td>
<td>TVD</td>
<td>-</td>
<td>85</td>
<td>ns</td>
<td>( TDD = 10.5V )</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>100</td>
<td>ns</td>
<td>( TDD = 9V )</td>
<td></td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>160</td>
<td>ns</td>
<td>( TDD = 4.75V )</td>
<td></td>
</tr>
<tr>
<td>( \text{A,B} ) inputs:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pulse Width</td>
<td>TPW</td>
<td>TVD+TOW</td>
<td>Infinite</td>
<td>ns</td>
<td>-</td>
</tr>
<tr>
<td>Phase Delay</td>
<td>TPS</td>
<td>TOW</td>
<td>Infinite</td>
<td>ns</td>
<td>-</td>
</tr>
<tr>
<td>( \text{A,B} ) frequency</td>
<td>fA,B</td>
<td>-</td>
<td>( \frac{1}{2TPW} )</td>
<td>Hz</td>
<td>( TOW &lt; TDD )</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>( \frac{1}{4TOW} )</td>
<td>Hz</td>
<td>( TOW \geq TDD )</td>
<td></td>
</tr>
</tbody>
</table>

Input to Output Delay

- \( \text{TDS} \) \( 120 \) \( ns \) \( VDD = 10.5V \) |
- \( \text{TDS} \) \( 150 \) \( ns \) \( VDD = 9V \) |
- \( \text{TDS} \) \( 235 \) \( ns \) \( VDD = 4.75V \) \( \text{Includes input validation delay} \) |

Output Clock Pulse Width

- \( \text{TOW} \) \( 50 \) \( ns \) \( \text{See Fig. 4 & 5} \)
FIGURE 2. LS7083/LS7084 INPUT/OUTPUT TIMING DIAGRAM

FIGURE 3. LS7083/LS7084 BLOCK DIAGRAM

The information included herein is believed to be accurate and reliable. However, LSI Computer Systems, Inc. assumes no responsibilities for inaccuracies, nor for any infringements of patent rights of others which may result from its use.
Figure 4. Tow vs RBIAS, \( K_\Omega \)

Figure 5. Tow vs RBIAS, \( M_\Omega \)

FIGURE 6A.
TYPICAL APPLICATION FOR LS7083 IN X4 MODE

FIGURE 6B.
TYPICAL APPLICATION FOR LS7084 WITH X4/X1 MODE SELECTION