

# Using Quadrature Encoders with E Series DAQ Boards

## Introduction

The DAQ-STC, the System Timing Controller device, is used on National Instruments E Series MIO DAQ boards as the timing engine for data acquisition and control operations. The DAQ-STC includes two general-purpose counter/timers that are useful for a wide variety of applications. This application note describes how you can use the DAQ-STC counter/timers to interface to quadrature encoders.

## Encoders

An encoder is a device that converts linear or rotary displacement into digital or pulse signals. The most popular type of encoder is the optical encoder, which consists of a rotating disk, a light source, and a photodetector (light sensor). The disk, which is mounted on the rotating shaft, has patterns of opaque and transparent sectors coded into the disk (see Figure 1). As the disk rotates, these patterns interrupt the light emitted onto the photodetector, generating a digital or pulse signal output.

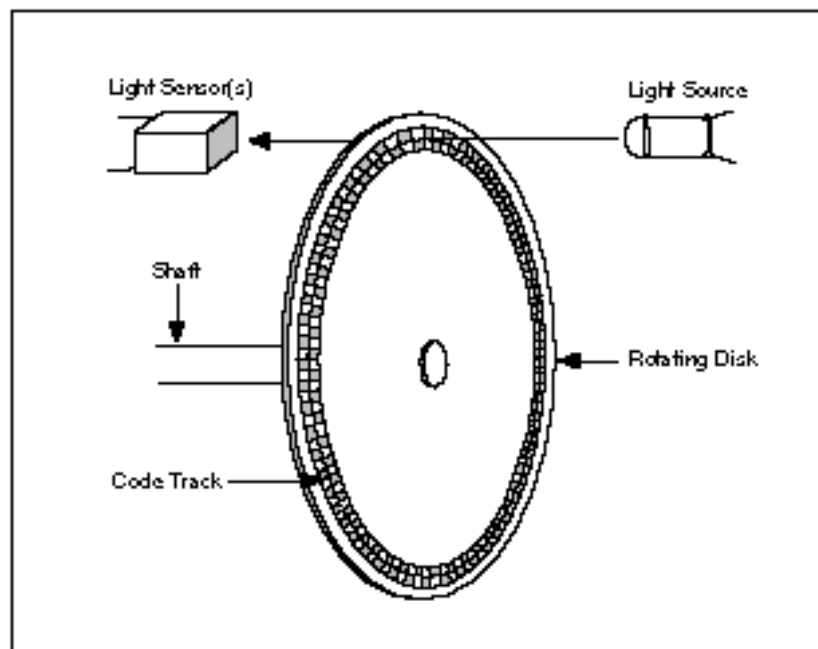


Figure 1. Optical Encoder

There are two general types of encoders – absolute and incremental encoders.

*Absolute Encoders* – An absolute encoder generates a unique word pattern for every position of the shaft. The tracks of the absolute encoder disk, generally four to six, commonly are coded to generate binary code, binary-coded decimal (BCD), or gray code outputs. Absolute encoders are most commonly used in applications where the device will be inactive for long periods of time, there is risk of power down, or the starting position is unknown.

*Incremental Encoders* – An incremental encoder generates a pulse, as opposed to an entire digital word, for each incremental step. Although the incremental encoder does not output absolute position, it does provide more resolution at a lower price. For example, an incremental encoder with a single code track, referred to as a tachometer encoder, generates a pulse signal whose frequency indicates the velocity of displacement. However, the output of the single-channel encoder does not indicate direction. To determine direction, a two-channel, or quadrature, encoder uses two detectors and two code tracks.

## Quadrature Encoders

The most common type of incremental encoder uses two output channels (A and B) to sense position. Using two code tracks with sectors positioned  $90^\circ$  out of phase (Figure 2), the two output channels of the quadrature encoder indicate both position and direction of rotation. If A leads B, for example, the disk is rotating in a clockwise direction. If B leads A, then the disk is rotating in a counter-clockwise direction. Therefore, by monitoring both the number of pulses and the relative phase of signals A and B, you can track both the position and direction of rotation.

In addition, some quadrature detectors include a third output channel, called a zero or reference signal, which supplies a single pulse per revolution. This single pulse can be used for precise determination of a reference position.

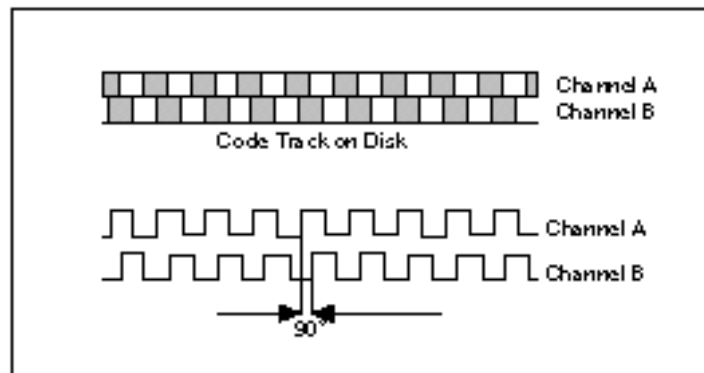


Figure 2. Quadrature Encoder Output Channels A and B

## The DAQ-STC Counter/Timer – An Overview

To meet the demands of today's high-performance data acquisition and control applications, National Instruments developed the Data Acquisition System Timing Controller (DAQ-STC), which integrates all data acquisition counter/timer functionality into a single ASIC. Designed primarily for use on multifunction input and output DAQ boards, the DAQ-STC includes 10 counter/timer devices, eight of which are designed to control the timing of analog input and analog output operations. The remaining two counter/timers are 24-bit up/down counter/timers available for a wide variety of timing and counting applications. The DAQ-STC is included on all National Instruments E Series MIO boards, including plug-in boards for ISA and PCI bus, and PCMCIA cards.

Each of the two 24-bit counter/timers of the DAQ-STC includes three input signals (SOURCE, GATE, and UP\_DOWN) and two output signals (OUT and INTERRUPT), as shown in Figure 3.

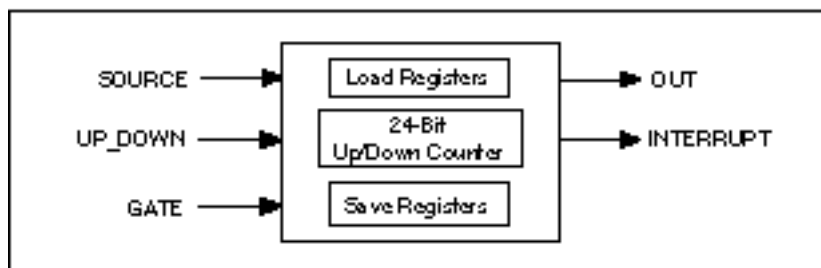


Figure 3. Simplified Counter/Timer Model of DAQ-STC

## Using Quadrature Encoders with the DAQ-STC

While the DAQ-STC includes a number of features useful for a large variety of timing and counting applications, its up/down counting feature is particularly convenient for encoders.

When using the DAQ-STC in event-counting mode, connect the pulse signal to be counted to the SOURCE input. When armed, the DAQ-STC count register increments (or decrements) on each transition at the SOURCE input (configurable for rising or falling edges). In addition, you can configure the DAQ-STC to count up, count down, or count up or down as determined by the state of the UP\_DOWN input.

When using quadrature encoders with the DAQ-STC, you have two choices. First, for simple applications, you can connect the encoder directly to the DAQ-STC, without any extra logic or signal conditioning. Although simple to implement, this configuration has the disadvantage of not being able to discern between stationary vibration of the encoder and real rotation. Second, you can interface the encoder to the DAQ-STC using a quadrature clock converter IC. This method prevents errors due to jitter and debouncing, and provides higher measurement resolution. These two methods are described below.

### Note on Signal Levels

The DAQ-STC, as well as the quadrature clock converter described here, provides TTL and CMOS compatible inputs and outputs. If your encoder provides outputs that are a different signal level, 24 V for example, then you may damage your equipment by connecting it directly to the DAQ-STC or clock converter. Therefore, you must either use an encoder that outputs TTL/CMOS signals, or use appropriate signal conditioning to convert the signal level and isolate the TTL/CMOS circuitry from high voltages. In either case, you may want to optically isolate your A and B signal lines to protect your DAQ board, PC, and operator from accidental application of high voltages.

## Method 1. Direct Connection to DAQ-STC (No Signal Conditioning)

For simple applications, you can connect quadrature encoders to the DAQ-STC counter/timer available on National Instruments E Series DAQ boards. By taking advantage of the UP\_DOWN control input, you can use the DAQ-STC to count up or down depending on the direction of shaft rotation.

To connect the encoder to the DAQ-STC, wire Channel A output of the encoder to the SOURCE input of the DAQ-STC and wire Channel B output of the encoder to the UP\_DOWN input. Figure 4 illustrates these connections for an AT-MIO-16E-2 board. Note that the UP\_DOWN input is accessed on the DIO6 pin for counter 0 or DIO7 for counter 1.

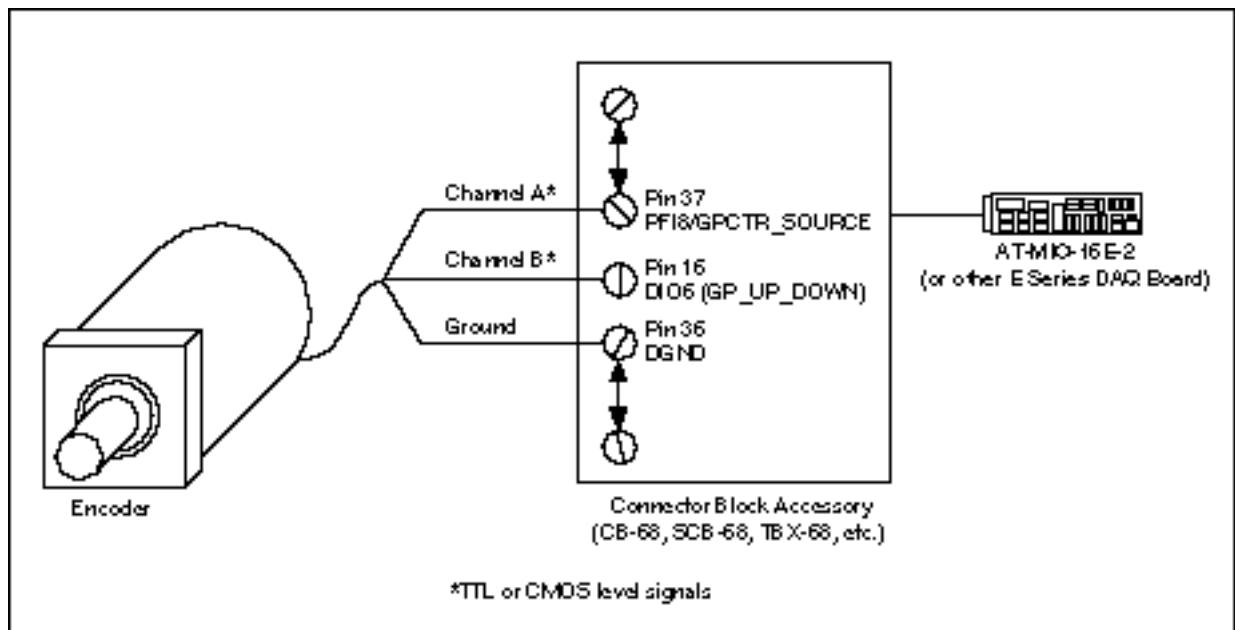


Figure 4. Direct (Nonconditioned) Encoder Connection to E Series DAQ Board

In this configuration, the counter will increment on state transitions (default low-to-high) on Channel A. When a Channel A low-to-high transition occurs, the state of Channel B will be high or low, depending directly on the direction of rotation. Therefore, the DAQ-STC counter will increment when the encoder rotates in one direction, and decrement when the encoder rotates in the opposite direction.

## Limitations of Method 1

While the configuration described above is very simple to implement, this method has a couple of potentially serious drawbacks. If the encoder disk is not rotating, but is vibrating enough back and forth to cause active transitions on Channel A, then each movement will be incorrectly counted. The effect of this dither motion is illustrated in Figure 5. As the encoder disk moves back and forth across  $A_2$ , Channel B remains low but the DAQ-STC counter continues to increment the count, resulting in an incorrect position reading. The quadrature clock converter device described in the next section solves this problem.

Another problem results when encoder outputs include noise or jitter that is large enough to be erroneously counted as a valid state transition. You can solve this problem with lowpass filters on the A and B signal outputs.

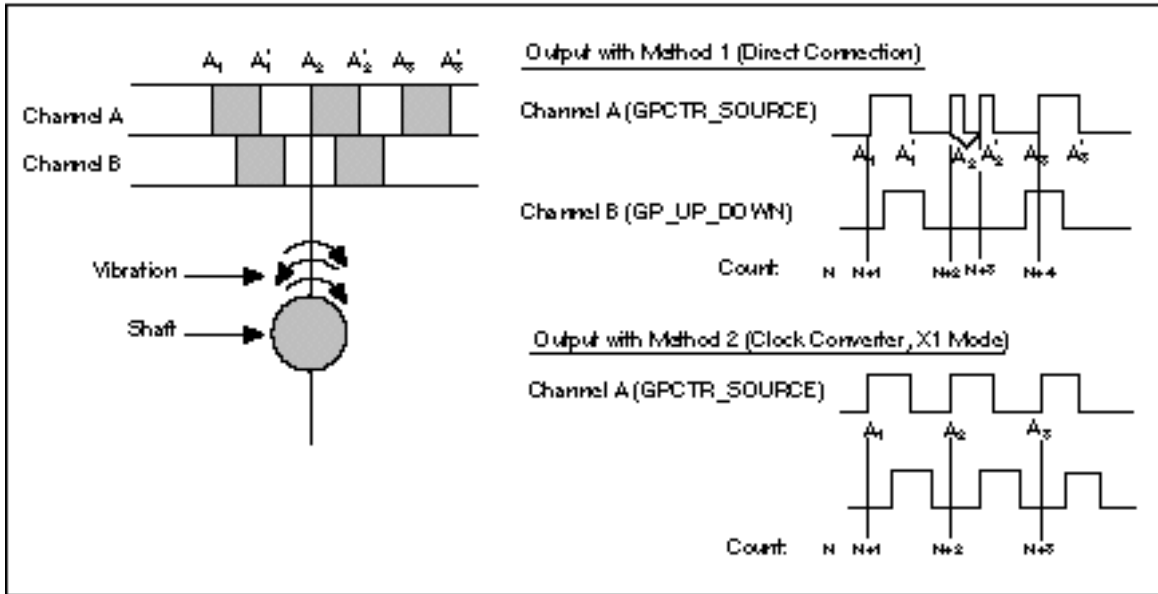


Figure 5. Dithering Effect of Vibration

## Method 2. Using Clock Converter with DAQ-STC for Reliable Measurements

You can greatly improve the reliability and quality of encoder measurements by using a clock converter device that conditions the encoder signals to prevent errors due to vibration, noise, and jitter. For example, the LS7084 quadrature clock converter from LSI Computer Systems, Inc. converts the A and B signals from an encoder into a clock and up/down signal that you can connect directly to the DAQ-STC. The LS7084 includes lowpass filters to prevent miscounts due to noise and jitter. In addition, the LS7084 uses dual one-shots to prevent the miscounting produced by vibration, or dither, as described in the previous section. The complete data sheet, with timing diagrams, is included at the end of this application note.

As shown in Figure 2 of the LS7084 data sheet (page 10), the CLK output, when in X4 mode, will pulse once on every transition of either the A or B signals. The UP/DN output indicates the direction of rotation. You can connect the A and B signals from a quadrature encoder directly to the LS7084, and connect the CLK and UP/DN outputs directly to the SOURCE and UP\_DOWN inputs of the DAQ-STC. Figure 6 illustrates the connections.

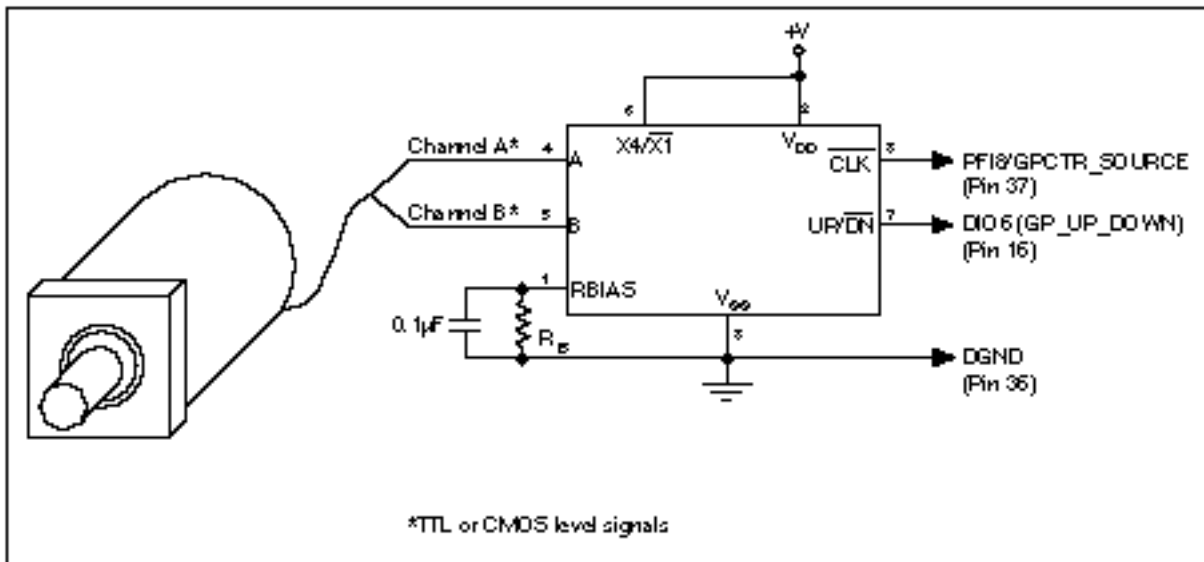


Figure 6. Encoder Connection to DAQ-STC using LS7084 Clock Converter

The value of the bias resistor,  $R_B$ , controls the pulse width of the CLK output. A 100 k $\Omega$  resistor will produce a pulse width of about 400 ns when using a voltage supply,  $V_{DD}$ , of 5 VDC.

## Using Encoders with 9513 or 8253/8254 Counter/Timers

The up/down counting feature of the DAQ-STC is very useful for quadrature encoders. The AM9513 and 8253/8254 counter/timers, used on some MIO Series and Lab/1200 Series DAQ products, do not include up/down counting capabilities. However, you may be able to use the LS7083, which is similar to the LS7084, to interface to encoders with these counter/timers. Similar to the LS7084, the LS7083 output signals include a UPCK signal which pulses when the encoder is rotating in the up direction, and a DNCK signal which pulses when the encoder is rotating in the down direction. By connecting these two output signals to the source or clock pins of two distinct counters on an AM9513 or 8253/8354, you can determine the total rotation by determining the difference between the two counts. One drawback of this method is that you must monitor the counts to determine when a counter hits full count and rolls over, so that the difference calculation is not distorted.

# Software

You control and use National Instruments DAQ products with NI-DAQ, a software driver that you can use with LabVIEW, LabWindows/CVI, ComponentWorks, or a third-party programming language. NI-DAQ includes function calls to use the DAQ-STC device for counting and timing.

*LabVIEW* – The **How to Count.vi** example that is included with the LabVIEW package includes several programming examples for counting applications with the DAQ-STC. Counting method number 3, “count up and down”, can be used with the quadrature encoder setups described in this application note. In short, this method enables the up/down counting by setting the count direction parameter in the CTR MODE CONFIG function to a value of 3.

*LabWindows/CVI and NI-DAQ* – When using LabWindows/CVI, or NI-DAQ with other programming languages, you program the DAQ-STC with GPCTR function calls. In particular, to configure a DAQ-STC counter for up/down counting, use the *GPCTR\_Change\_Parameter* function with parameter type set to ND\_UP\_DOWN and parameter value set to ND\_HARDWARE.

Once the DAQ-STC is properly configured and your software program correctly retrieves the count from the counter, you can convert the count into rotation by using one of the following simple formulas:

With LS7804 in X4 Mode:

$$\text{Amount of Rotation (}^\circ\text{)} = \frac{\text{Count}}{4N} \times 360^\circ$$

With LS7804 in X1 Mode, or with no extra circuitry:

$$\text{Amount of Rotation (}^\circ\text{)} = \frac{\text{Count}}{N} \times 360^\circ$$

where N = number of cycles or pulses produced by encoder per shaft rotation.

## QUADRATURE CLOCK CONVERTER

April 1995

### FEATURES:

- X1 and X4 mode selection
- Up to 16 MHz output clock frequency
- Programmable output clock pulse width
- On-chip filtering of inputs for optical or magnetic encoder applications.
- TTL and CMOS compatible I/Os
- +4.75V to +10.5V operation (VDD-VSS)
- 8-Pin DIP (SOIC available)

### DESCRIPTION:

The LS7083 and LS7084 are monolithic CMOS silicon gate quadrature clock converters. Quadrature clocks derived from optical or magnetic encoders, when applied to the A and B inputs of the LS7083/LS7084, are converted to strings of Up Clocks and Down Clocks (LS7083) or to a Clock and an Up/Down direction control (LS7084). These outputs can be interfaced directly with standard Up/Down counters for direction and position sensing of the encoder.

### INPUT/OUTPUT DESCRIPTION:

#### RBIAS (Pin 1)

Input for external component connection. A resistor connected between this input and Vss adjusts the output clock pulse width (Tow). For proper operation, the output clock pulse width must be less than or equal to the A,B pulse separation ( $TOW \leq T_{PS}$ ).

#### VDD (Pin 2)

Supply Voltage positive terminal.

#### VSS (Pin 3)

Supply Voltage negative terminal.

#### A (Pin 4)

Quadrature Clock Input A. This input has a filter circuit to validate input logic level and eliminate encoder dither.

#### B (Pin 5)

Quadrature Clock Input B. This input has a filter circuit identical to input A.

#### X4/X1 (Pin 6)

This input selects between X1 and X4 modes of operation. A high-level selects X4 mode and a low-level selects the X1 mode. In X4 mode, an output pulse is generated for every transition at either A or B input. In X1 mode, an output pulse is generated in one combined A/B input cycle. (See Figure 2.)

### PIN ASSIGNMENT - TOP VIEW STANDARD 8 PIN PLASTIC DIP

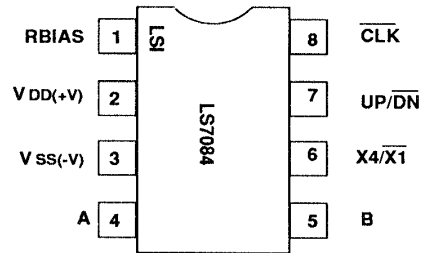
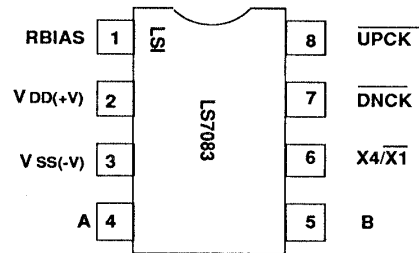


FIGURE 1

#### LS7083 - $\overline{DNCK}$ (Pin 7)

In LS7083, this is the DOWN Clock Output. This output consists of low-going pulses generated when A input lags the B input.

#### LS7084 - $UP/\overline{DN}$ (Pin 7)

In LS7084, this is the count direction indication output. When A input leads the B input, the  $UP/\overline{DN}$  output goes high indicating that the count direction is UP. When A input lags the B input,  $UP/\overline{DN}$  output goes low, indicating that the count direction is DOWN.

#### LS7083 - $\overline{UPCK}$ (Pin 8)

In LS7083, this is the UP Clock output. This output consists of low-going pulses generated when A input leads the B input.

#### LS7084 - $\overline{CLK}$ (Pin 8)

In LS7084, this is the combined UP Clock and DOWN Clock output. The count direction at any instant is indicated by the  $UP/\overline{DN}$  output (Pin 7).

**NOTE:** For the LS7084, the timing of  $\overline{CLK}$  and  $UP/\overline{DN}$  requires that the counter interfacing with LS7084 counts on the rising edge of the  $\overline{CLK}$  pulses.



**ABSOLUTE MAXIMUM RATINGS:**

PARAMETER	SYMBOL	VALUE	UNITS
DC Supply Voltage	VDD - VSS	12	V
Voltage at any input	VIN	VSS - .3 to VDD +.3	V
Operating temperature	TA	0 to +70	°C
Storage temperature	TSTG	-55 to +150	°C

**DC ELECTRICAL CHARACTERISTICS:**

(All voltages referenced to VSS, TA = 0°C to 70°C.)

PARAMETER	SYMBOL	MIN	MAX	UNITS	CONDITION
Supply voltage	VDD	4.75	10.5	V	-
Supply current	IDD	-	6.0	μA	VDD = 10.5V, All input frequencies = 0 Hz RBIAS = 2MΩ
<b>X4/X1</b> Logic Low	VIL	-	-	0.3VDD	V
<b>A,B</b> Logic Low	VIL	-	0.6	V	VDD = 4.75V
		-	1.0	V	VDD = 9V
		-	1.1	V	VDD = 10.5V
<b>X4/X1</b> Logic High	VIH	0.7VDD	-	V	-
<b>A,B</b> Logic High	VIH	3.1	-	V	VDD = 4.75V
		5.0	-	V	VDD = 9V
		5.6	-	V	VDD = 10.5V
<b>ALL OUTPUTS:</b>					
Sink Current	IOL	1.75	-	mA	VDD = 4.75V
VOL = 0.4V		5.0	-	mA	VDD = 9V
		5.7	-	mA	VDD = 10.5V
Source Current	IOH	1.0	-	mA	VDD = 4.75V
VOH = VDD - 0.5V		2.5	-	mA	VDD = 9V

**TRANSIENT CHARACTERISTICS:**

(TA = 0°C to 70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	CONDITION
<b>A,B</b> inputs:					
Validation Delay	TvD	-	85	ns	VDD = 10.5V
		-	100	ns	VDD = 9V
		-	160	ns	VDD = 4.75V
<b>A,B</b> inputs:					
Pulse Width	TPW	TDD+TOW	Infinite	ns	-
<b>A to B</b> or <b>B to A</b>					
Phase Delay	TPS	TOW	Infinite	ns	-
<b>A,B</b> frequency	fA,B	-	$\frac{1}{2TPW}$	Hz	TOW < TDD
		-	$\frac{1}{4TOW}$	Hz	TOW ≥ TDD
Input to Output Delay	TDS	-	120	ns	VDD = 10.5V
		-	150	ns	VDD = 9V
		-	235	ns	VDD = 4.75V Includes input validation delay
Output Clock Pulse Width	TOW	50	-	ns	See Fig. 4 & 5

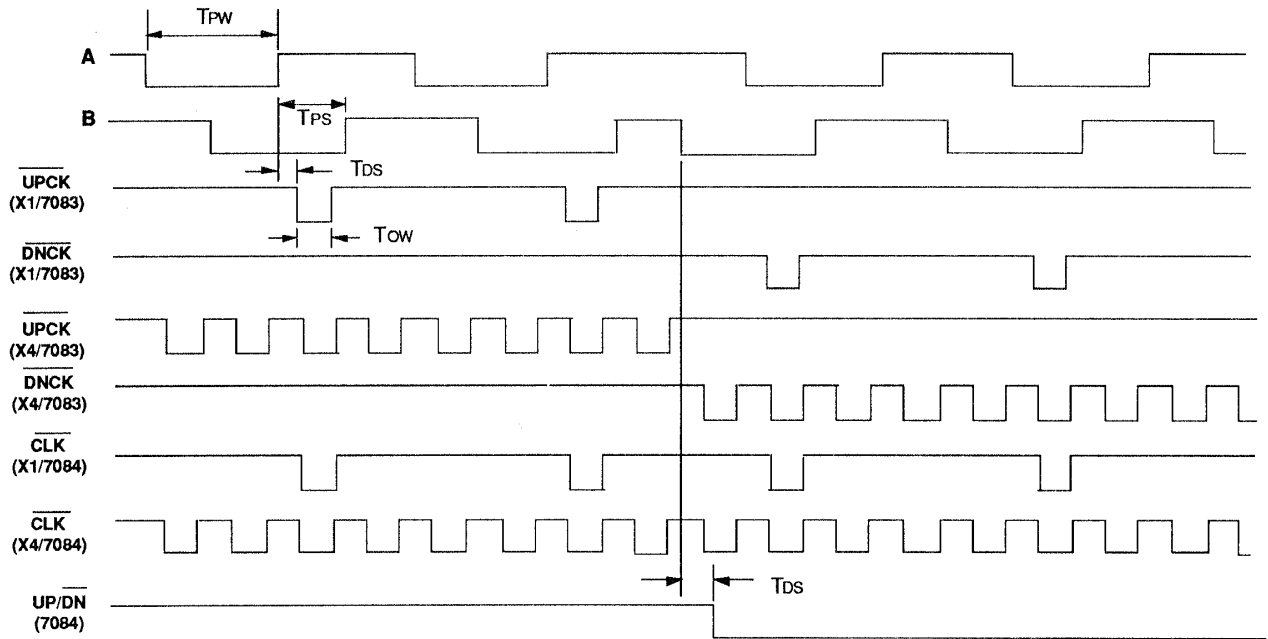


FIGURE 2. LS7083/LS7084 INPUT/OUTPUT TIMING DIAGRAM

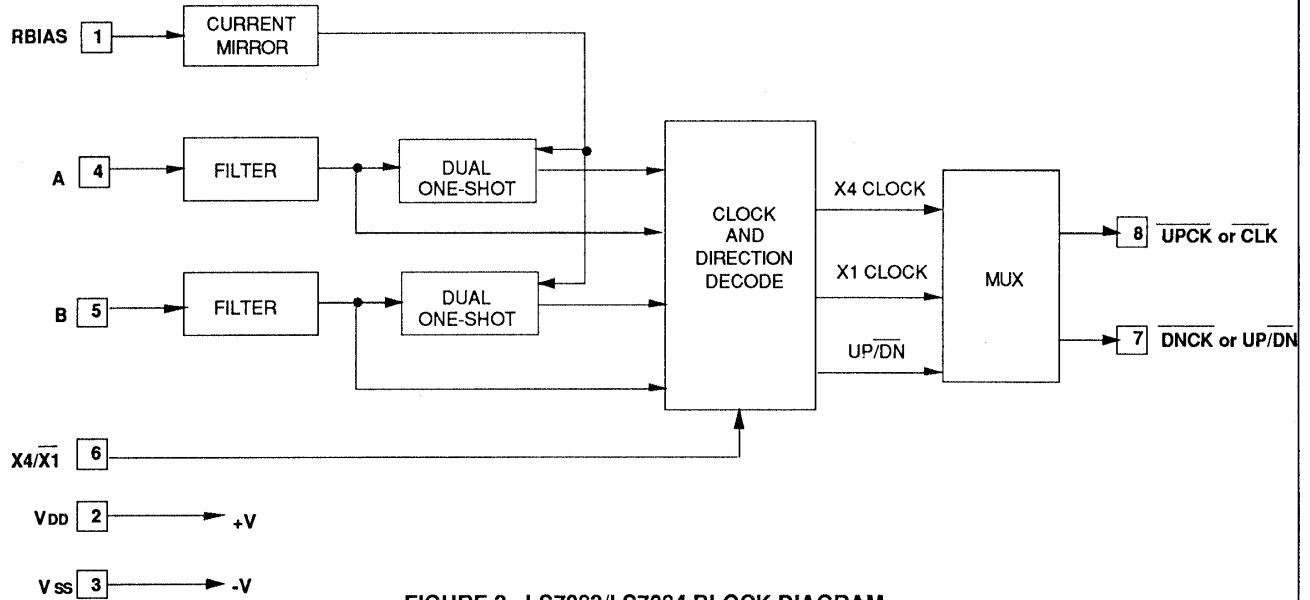


FIGURE 3. LS7083/LS7084 BLOCK DIAGRAM

The information included herein is believed to be accurate and reliable. However, LSI Computer Systems, Inc. assumes no responsibilities for inaccuracies, nor for any infringements of patent rights of others which may result from its use.

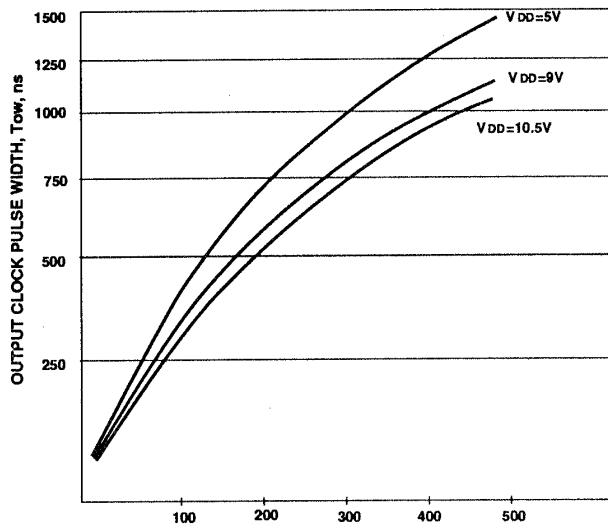


Figure 4. TOW vs RBIAS, KΩ

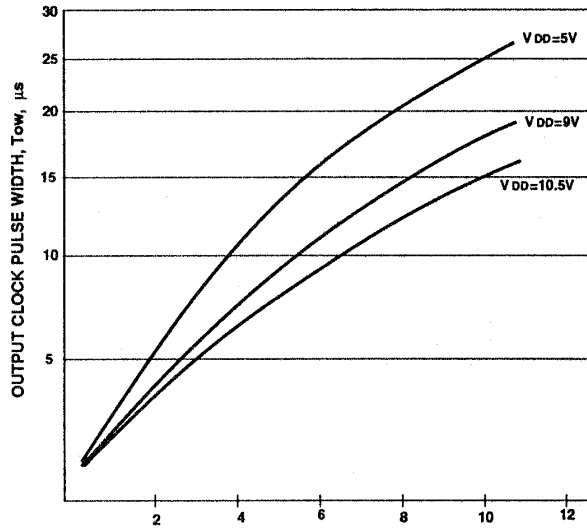


Figure 5. TOW vs RBIAS, MΩ

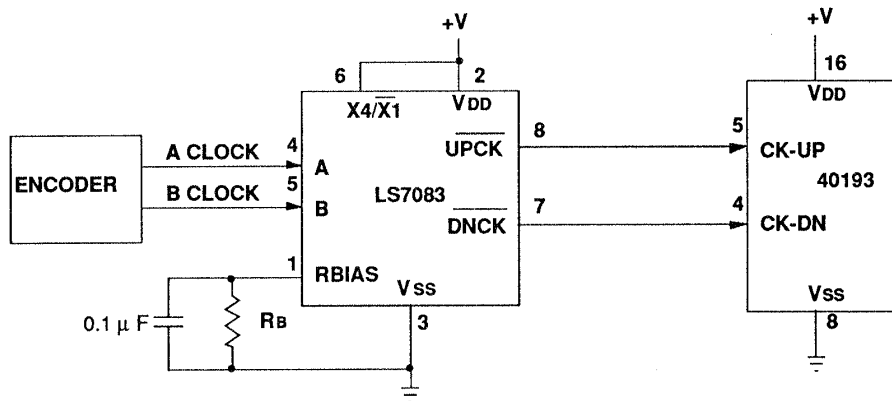


FIGURE 6A.  
TYPICAL APPLICATION FOR LS7083 IN X4 MODE

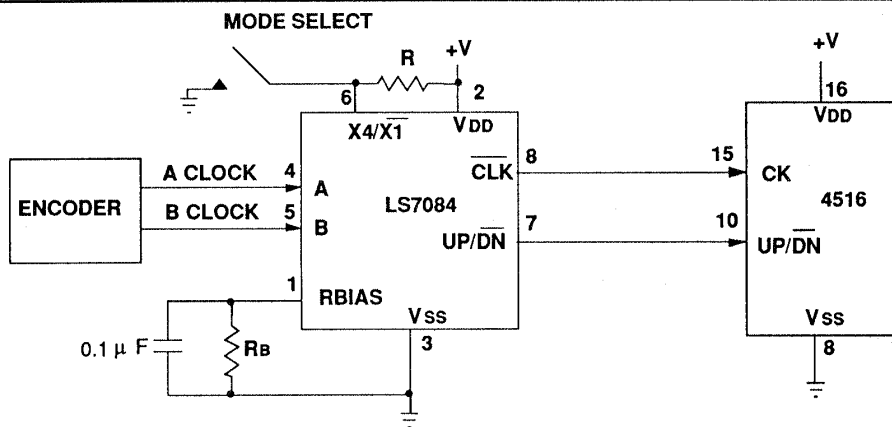


FIGURE 6B.  
TYPICAL APPLICATION FOR LS7084 WITH X4/X1 MODE SELECTION