Even though we demonstrated how to group 0s and write the corresponding product-of-sums functional forms for four-variable Karnaugh maps, it should be obvious that essentially the same technique can be employed for three-variable maps. The details are left as exercises in the following problem set.

SUMMARY

1. The representation of a number depends upon the base of the number system selected.

2. Arithmetic can be performed in the binary number system as well as the decimal number system.

3. Nonnumerical information can be put in binary form by using codes.

4. The position of a switch (i.e., open, closed) in a circuit can be characterized by the binary digits (bits) 0 and 1.

5. AND, OR, NOT (complement), exclusive-OR, NAND, and NOR operations are examples of logic operations.

6. Logic gates are circuits that perform logic operations.

7. Switching or logic circuits are characterized by Boolean functions.

8. Boolean functions can be manipulated by using the rules of Boolean algebra.

9. Boolean functions in standard form can be implemented with two-level logic.

10. NAND and NOR gates are universal gates—either type can be used exclusively to realize arbitrary Boolean functions.

11. Boolean functions can be simplified graphically by using Karnaugh maps.

12. Grouping the 1s on a Karnaugh map produces a simplified sum-of-products expression, whereas grouping the 0s yields a simplified product-of-sums functional form.

PROBLEMS

11.1 Make a list of the binary numbers from zero to fifteen.

11.2 Express the following binary numbers in decimal form: (a) 11011, (b) 101011, (c) 0.11011, (d) 0.10101, (e) 10100.011, (f) 10011.101.

11.3 Express the following decimal numbers in binary form: (a) 43, (b) 27, (c) 0.84375, (d) 0.65625, (e) 19.625, (f) 20.375.

11.4 Express the following octal numbers in decimal form: (a) 33, (b) 53, (c) 0.66, (d) 0.52, (e) [illegible], (f) 23.5.

11.5 Express the following decimal numbers in octal form: (a) 43, (b) 27, (c) 0.84375, (d) 0.65625, (e) 19.625, (f) 20.375.

11.6 Express the following binary numbers in octal form: (a) 110010110.1, (b) 101100101.01, (c) 11101001.111.

11.7 Express the following octal numbers in binary form: (a) 20.375, (b) 413.702, (c) 2610.35.

11.8 Repeat Problem 11.6 converting from binary to hexadecimal numbers.

(4K-bit) RAM that has the form shown in (a) Fig. 13.26 on p. 880 and (b) Fig. 13.27 on p. 881. How many inputs does each AND gate have?

13.25 Each of 40 tracks of a $5\frac{1}{4}$-inch floppy disk is partitioned into 9 sectors—each containing 512 bytes (1 byte = 8 bits). Determine the information-storage content of this floppy disk. What is the information-storage content if the number of tracks is increased to 80?

13.26 Extend the waveforms ϕ_1, ϕ_2, and ϕ_3 shown in Fig. 13.35 on p. 888 and add the waveform for ϕ_4 such that the packet of charge under gate ϕ_3 is shifted to the right to the next gate labeled ϕ_1. (The device that produces waveforms ϕ_1, ϕ_2, ϕ_3, and ϕ_4 is known as a **four-phase clock.**)

13.27 For the 3-bit DAC shown in Fig. 13.37 on p. 892, suppose that $R_1 = 7R_F$, and $R_2 = 10R$. Construct a table indicating the output voltages that correspond to the eight possible 3-bit binary inputs, given that a logical 0 and a logical 1 correspond to 0 V and 1 V, respectively.

13.28 For the 3-bit DAC shown in Fig. 13.37 on p. 892, suppose that $R_1 = R_F$ and $R_2 = R$. Construct a table indicating the output voltages that correspond to the eight possible 3-bit binary inputs, given that a logical 0 has the value 0 V and a logical 1 has the value 1.5 V.

13.29 Based on the DAC shown in Fig. 13.37 on p. 892, design a 4-bit DAC whose maximum output voltage is 10 V, given that a logical 0 and a logical 1 correspond to 0 V and 1 V, respectively.

13.30 For the 3-bit DAC shown in Fi[illegible] suppose that $R_2 = 17R_1$. Construct a tab[illegible] the output voltages that correspond to the [illegible] sible 3-bit binary inputs, given that a logic[illegible] logical 1 correspond to 0 V and 1 V, respe[illegible]

13.31 Repeat Problem 13.29 for the D[illegible] in Fig. 13.38 on p. 892.

13.32 The DAC shown in Fig. P13.3[illegible] prised of three individual DACs. For the [illegible] on the left, when the input is the binary [illegible] tion of the decimal digit D, the output [illegible] Express R_0 and R_1 in terms of R_F and R [illegible] when the input of the overall DAC is the [illegible] number D_1D_0, the output that results is v_2 = [illegible] volts.

13.33 For the 2-bit parallel-compara[illegible] shown in Fig. 13.41 on p. 895, suppose [illegible] and the analog input voltage varies betw[illegible] 8 V. Determine the input-voltage interval [illegible] responds to a digital output B_1B_0 of (a) [illegible] (c) 10, and (d) 11.

13.34 Draw a 3-bit parallel-compara[illegible] Construct the truth table relating the enco[illegible] and outputs.

13.35 Given an n-bit ADC whose ana[illegible] voltage varies over a range of V_r volts, the re[illegible] of the ADC is defined to be $V_r/2^n$. In terms [illegible] percentage of V_r, the resolution is $1/2^n$. De[illegible] the resolution of an n-bit ADC for the [illegible] (a) $n = 2$, (b) $n = 3$, (c) $n = 4$, (d) n = [illegible] (e) $n = 8$.

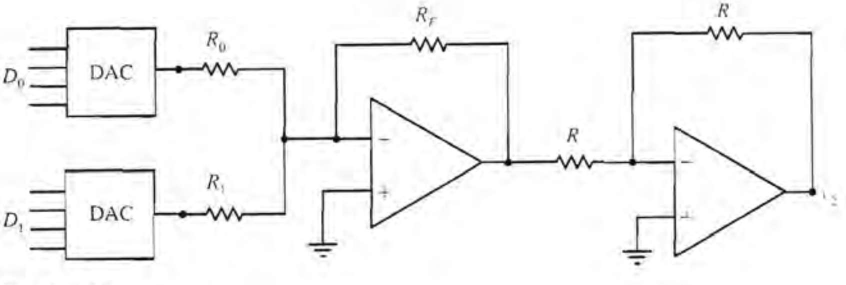

Fig. P13.32

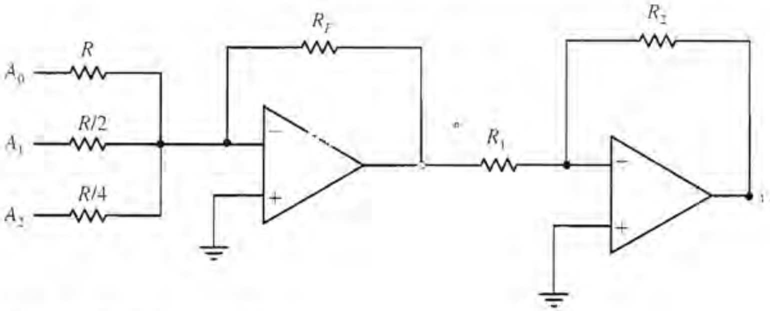

Fig. 13.37 A 3-bit DAC.

Consider the case that $R_1 = R_F$ and $R_2 = R$. Then we have

$$v_2 = 4A_2 + 2A_1 + A_0$$

Under this circumstance, when the input is $A_2A_1A_0 = 000$, the output is $v_2 = 0$ V; whereas when the input is $A_2A_1A_0 = 111$, the output is $v_2 = 7$ V. In general, for these choices of R_1 and R_2, the value of the output voltage is equal to the value of the binary number put in. Different choices for R_1 and R_2 will result in different output voltages (see Problem 13.27 at the end of this chapter). Further, if logical 0 and logical 1 correspond to voltages other than 0 V and 1 V, respectively, different output voltages will again result (see Problem 13.28 at the end of this chapter).

Extending the circuit shown in Fig. 13.37 to implement a DAC with more than three input bits requires additional input resistors $R/8$, $R/16$, $R/32$, and so on (see Problem 13.29 at the end of this chapter). Because of the wide variation of input-resistance values required for DACs with many input bits, a better DAC design is the one shown in Fig. 13.38. This DAC uses a connection of resistors called an ***R*-2*R* ladder**, and employs a single op amp.

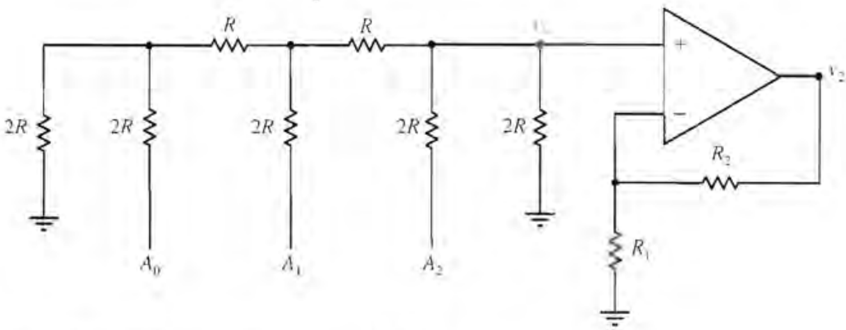

Fig. 13.38 A 3-bit DAC using an *R*-2*R* ladder.